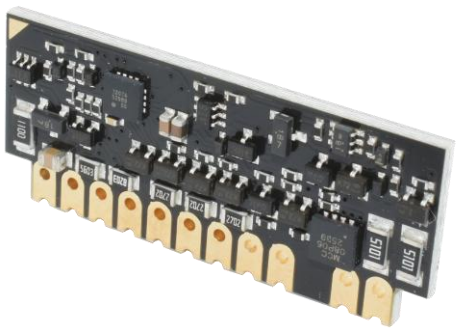
Silvertel

Ag59FE

Power-over-Ethernet Configurable PD Controller Module



Features

- Configurable Power Classification, from Class 0 to Class 8
- IEEE802.bt, IEEE802.3at, & IEEE802.3af compliant
- 'Power Good' Output
- Line Power Pass-through Output
- PoE Disable function
- Maintain Power Signature for low power applications
- Industrial temperature range
- Minimal external components required
- Flexi-format Single-in-Line (SIL) or SMT package 35mm(L) x 14mm(H)
- Silvertel technical "design-in" assistance
- Designed and Manufactured in the UK

Description

The Ag59FE module is a Power-over-Ethernet Powered Device (PD) Controller module, which can be paired with a DC/DC converter to provide a complete PoE solution.

Designed to extract power from a conventional twisted pair Category 5 Ethernet cable, conforming to the IEEE802.3 PoE standard, with full compatibility with the IEEE802.3af, IEEE802.3at and IEEE802.3bt amendments.

The Ag59FE can be configured as a Type 1, 2, 3 or 4, Class 0-8 PD device, requesting up to 90W of power from the PSE.

When used in conjunction with an isolated DC/DC converter, constant current circuit, or enclosure, the application is capable of being configured as a fully compliant PD solution providing a DC voltage to the connected peripheral device.

Typical applications include PoE lighting, Ethernet extenders and media converters.

Table of Contents

Table of Figures

1 Product Overview

1.1 Ag59FE Product Selector

Part Number[1]	Marking[2]	Package
Ag59FE	abc	SIL / SMT[3]

Table 1: Ordering Information

Note 1: Complies with the European Directive 2011/65/EU for the Restriction of use of certain Hazardous Substances (RoHS) including Directive 2015/863 published in 2015, amending Annex II of Directive 2011/65/EU. Moisture Sensitive Level 1 and HBM 1.

Note 2: Located on the rear of the module.
The first letter, a, indicates the week as A-Z with uppercase being weeks 1-26, lower case weeks 27-52.
The second letter, b, indicates the year in uppercase A-Z starting from 2020.
The final letter, c, is a Silvertel reference.

Note 3: See Figure 11 for details on how Ag59FE can be used as a SIL or SMT device.

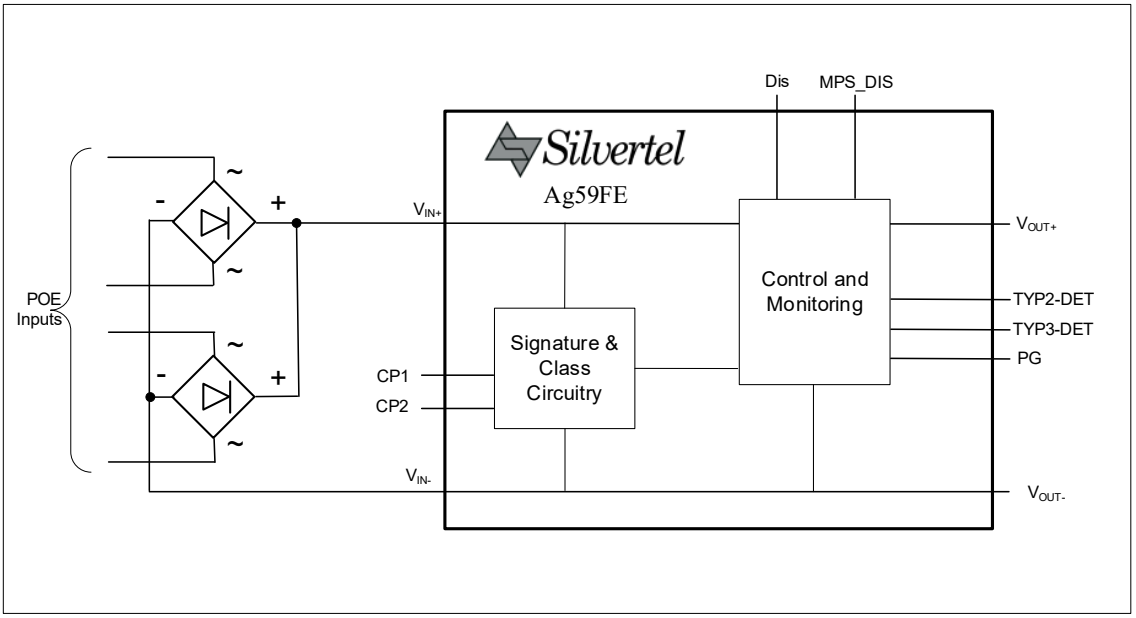


Figure 1: Block Diagram

1.2 Package Format

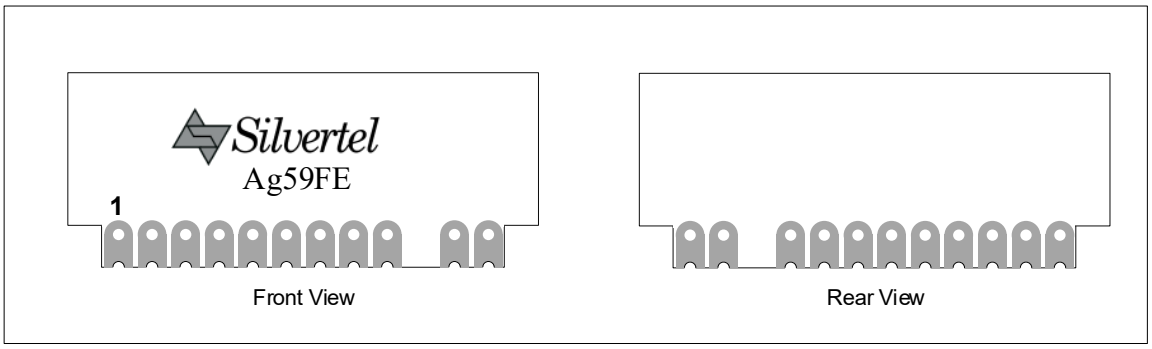


Figure 2: Ag59FE Package Format

1.3 Pin Description

Pin #	Name	Description
1	V_{IN+}	**POE Direct Input +.** This pin connects to the positive (+) output of the POE input bridge rectifiers.
2	V_{IN-}	**POE Direct Input -.** This pin connects to the negative (-) output of the POE input bridge rectifiers.
3	MPS_Dis	**MPS Disable.** This pin can be pulled down to V_{IN-} to disable the MPS current draw; see Section 2.2 for more details.
4	CP1	**Class Programming.** These pins are used to configure the Classification request, see Section 2.3 for more details.
5	CP2	
6	TYP3_DET	**PoE Type Detection Output.** The combination of these pin outputs indicate the power level the PSE is supplying; can be used to determine whether the Ag59FE has sufficient power, see Section 2.4 for more details.
7	TYP2_DET	
8	PG	**Power Good Output.** This pin can be used for application power up sequencing. This pin Pulls down from V_{OUT+} after power up, see section 3.2 for more details.
9	Dis	**PoE Disable.** When Pulled LOW the Ag59FE disables its output and no longer presents a valid signal; see section 2.2 for more details.
10	V_{OUT-}	**Negative DC Output.** Internally connected to V_{in-}.
11	V_{OUT+}	**Positive DC Output.** This pin provides the positive output from the Ag59FE.

Table 2: Pin Description

1.4 Typical Connections

The Ag59FE only requires a few external components - the bridge rectifiers on the V_{IN} inputs are to conform to the input polarity protection requirement, and a form of overvoltage protection is recommended.

The input supply of the module will be passed through to the output after the negotiation has taken place and the module is powered. The bulk capacitor (C1) connected across the output is optional, it is recommended that any capacitor fitted is less than 180µF. See section 3.1 for more details.

The Power Good output can be used to prevent the application exceeding the power limitations of the specification during powerup by delaying the booting of any application circuitry, see section 3.2 for more details.

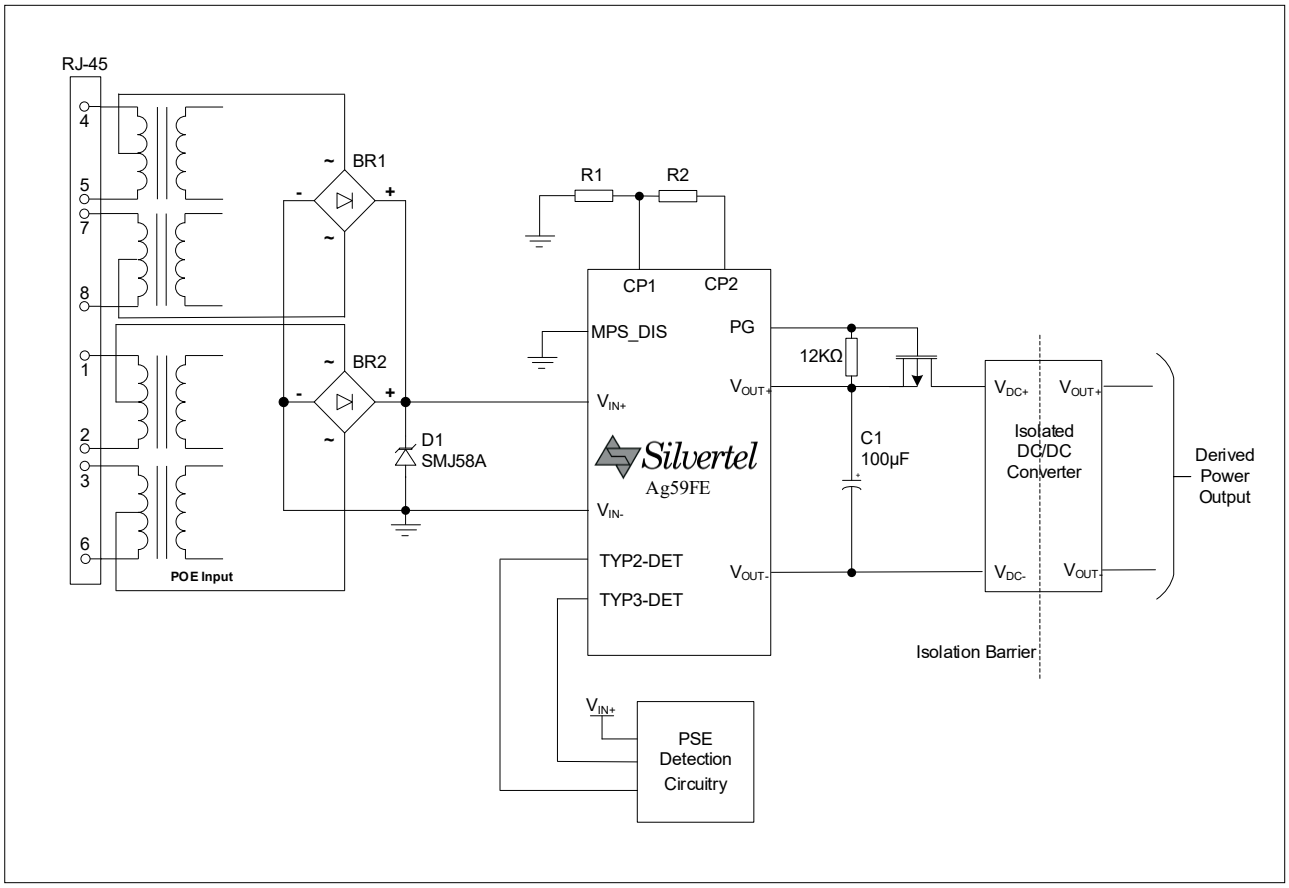


Figure 3: Typical System Diagram

2 Input

The Ag59FE has two power pins V_{IN+} and V_{IN-}, these should be connected to the outputs of two external bridge rectifiers (see Figure 3: Typical System Diagram). This allows the Ag59FE to be compatible with Power Sourcing Equipment (PSE) that utilise any of the permissible power source polarity configurations.

The Ag59FE is designed to be powered by any compliant IEEE802.3 PSE, such as Silvertel's Ag6810.

2.1 PD Signature

The Ag59FE complies with the IEEE802.3 specifications and provides the required signature and control circuitry within. When the inputs are connected to a PSE, they will automatically present a Powered Device (PD) signature to the PSE (when requested). The PSE will then recognise that a valid PD is connected to that line and progress to the classification and powering stages.

2.2 PoE Disable

In certain applications, where device power may come from an independent external supply, it can be desirable to disable the PoE functionality. If this is desired, pulling the DIS pin LOW will result in the module powering down, turning off the output and disabling the signature circuitry to prevent power cycling as a result of the PSE detecting the PoE signature.

2.3 Power Classification Programming

The Ag59FE is a programmable classification front end that can be configured to request any of the power level requests contained in the IEEE802.3 specification, for applications with a maximum power ranging from 4W to 90W. Table 3: Classification Table below shows the available power levels and the corresponding Class Pulse responses.

If the Ag59FE is connected to a PSE that cannot output the power request by the Ag59FE, the PSE will recognise the Class request as a valid request beyond maximum output and default to its highest output classification power level, supplying 15.4W for a type 1 PSE, 30W for a Type 2 PSE, or 60W for a Type 3 PSE.

Requested Class	Class Pulse Count	*Pulse 1&2 Classification Current (mA)*	Pulse 3+ Classification Current (mA)	PSE Output Power (W)	Min. Available PD Power (W)	IEEE Spec. Amendment
0	1	<5	N/A	15.4	12.75	802.3af
1	1	10	N/A	4	3.84	
2	1	20	N/A	7	6.49	
3	1	30	N/A	15.4	12.75	
4	2 or 3	40	40	30	25.5	802.3at
5	4	40	<5	45	40	802.3bt
6	4	40	10	60	51	
7	5	40	20	75	62	
8	5	40	30	90	71.3	

Table 3: Classification Table

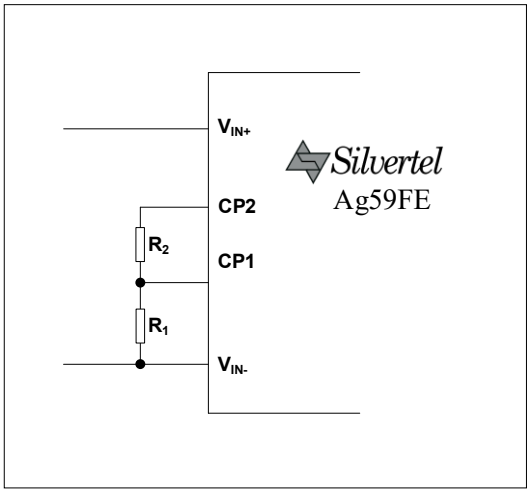


Figure 4: Classification Programming

Requested Class	R1 Value	R2 Value
0	Open Circuit	Open Circuit
1	910Ω	Open Circuit
2	430Ω	Open Circuit
3	270Ω	Open Circuit
4	180Ω	Open Circuit
5	Open Circuit	160Ω
6	910Ω	220Ω
7	430Ω	330Ω
8	270Ω	560Ω

Table 4: Configuring Classification

2.4 PSE Type Detection

The IEEE802.3 specification stipulates that if a device detects it is connected to a PSE that is not capable of providing the full requested power level, the device should remain in a reduced power mode and/or indicate to the user that the device is under powered. To complete the protocol (and conform to the IEEE802.3 specification) the controller should then confirm that it is greater than a Type 1 PD over the Data Link Layer if configured to class 4 or higher, see ANX-POE- Data Link Layer Classification for more details.

The Ag59FE monitors the detection and classification sequence to determine the power output of the connected PSE. The module features two type detection output pins, TYP2-DET and TYP3-DET, to flag the detected PSE Type.

The flagging can be used to adjust the peak power draw of the application or to inform the user that the device is under powered and may power cycle.

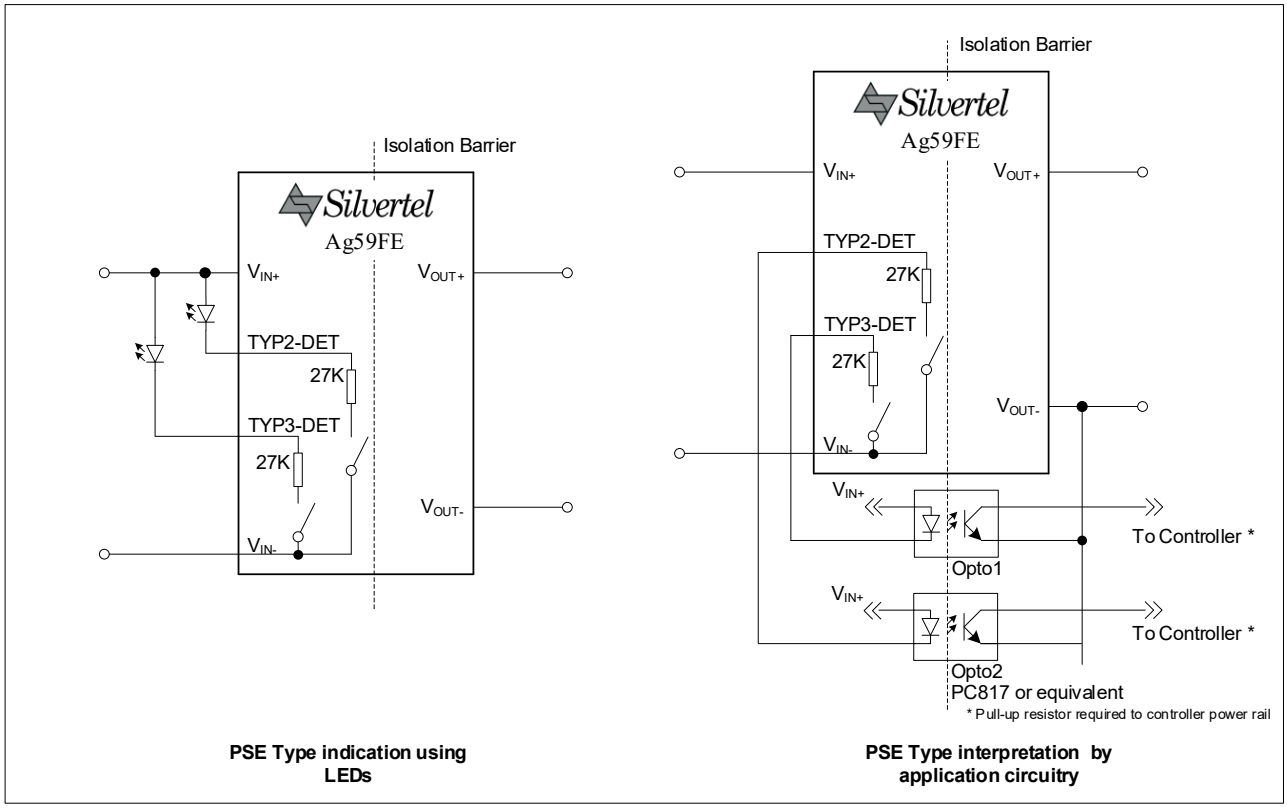


Figure 5: Physical Layer Detect Configuration

When the PSE type has been detected, the relevant pins will pull low from V_{in+}; this can be used to drive an LED or an Optocoupler as shown in Figure 5: Physical Layer Detect Configuration.

Detected PSE Type	Type2-DET Output	Type3-DET Output
1	High	High
2	Low	High
3	High	Low
4	Low	Low

Table 5: Type Detect Output Table

2.5 Maintain Power Signature

The Ag59FE does not require a load for operation. However, PoE does have a Maintain Power Signature (MPS) requirement as stipulated in the IEEE802.3 specification, to ensure that power is not being supplied to an unconnected port.

When the PSE detects that the MPS requirement is not being met it will remove power from the port. If the applications load on the module drops below I_{OUT_MPS} (see section 11.2) for a length of time greater than 250ms (pulses less than 75ms in duration are ignored), the PSE may determine that the device has been disconnected.

To prevent this, the Ag59FE can apply a pulsed load to the ethernet link to satisfy the MPS requirement while minimising power consumption. If the PSE has indicated it supports the low power MPS introduced in the IEEE802.3bt amendment, the Ag59FE will automatically change to the low power profile for the pulsed load to further reduce power consumption.

This pin can either be controlled by use of a zero ohm link to permanently disable the MPS load, or dynamically controlled by a controller to only apply the MPS load when the application is in a low power state.

To disable the MPS pulsed load the MPS_DIS pin should be pulled LOW, otherwise the Ag59FE will apply this loading while the MPS_DIS pin is left floating.

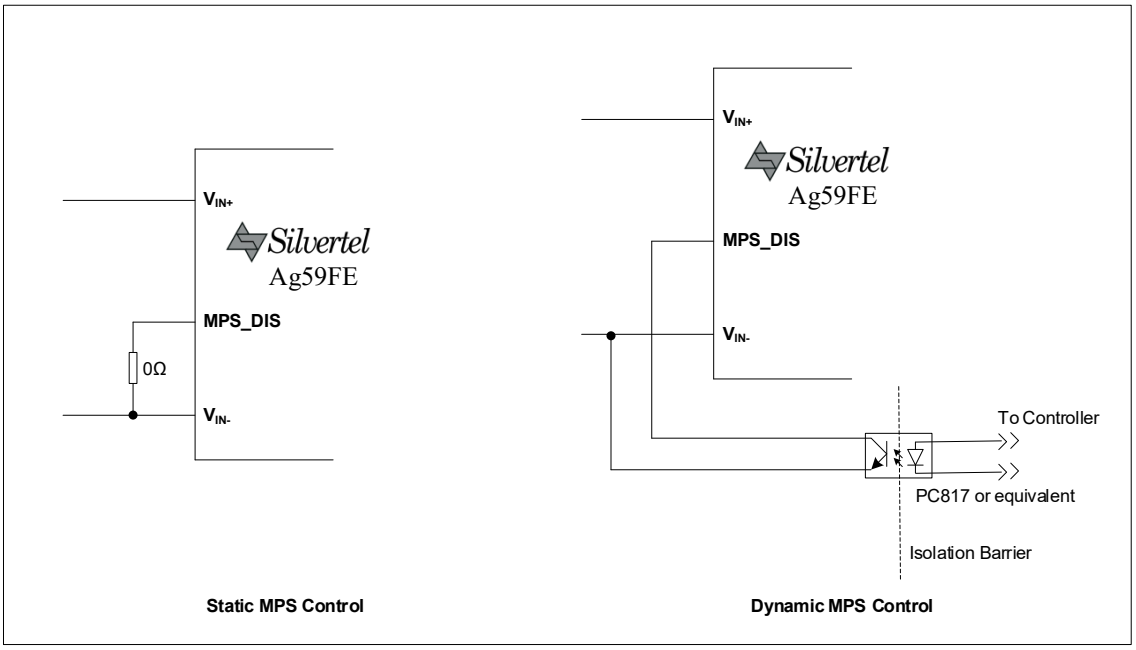


Figure 6: MPS Control

3 Output

3.1 Output Capacitance

The Ag59FE does not require any bulk capacitance on the output, but some capacitance may be beneficial to the application.

When a PoE PD is first powered, the inrush currents should be controlled to prevent damage to the equipment. The PSE will impose a 400mA current limit on each powered pairset as it raises the voltage of the port to transmission voltage. If the capacitance on the directly on the output of the Ag59FE is greater than 180µF the PD may not be up to the operational voltage before the inrush timer elapses, this could lead to the PSE's protections resulting in the removing of power from the link.

The combined value of capacitance directly on the output of the Ag59FE should not exceed 180µF, unless capacitor inrush currents are limited.

3.2 Power Good

To reduce the risk of start-up issues due to overloading, it is recommended to use the Power Good output to sequence any DC/DC converters on the output.

One simple method of implementing this is by use of a P-Channel MOSFET rated for the peak currents expected by the application load, this is ideal for applications where the PoE transmission voltages are required.

Alternatively, the Power Good Output can be used to the drive any enable or control input of the applications DC/DC converter, depending on the topology of the DC/DC converter being implemented, additional circuitry may be required to drive the control pin correctly. The PG pin is pulled low with a 27KΩ pull down resistance.

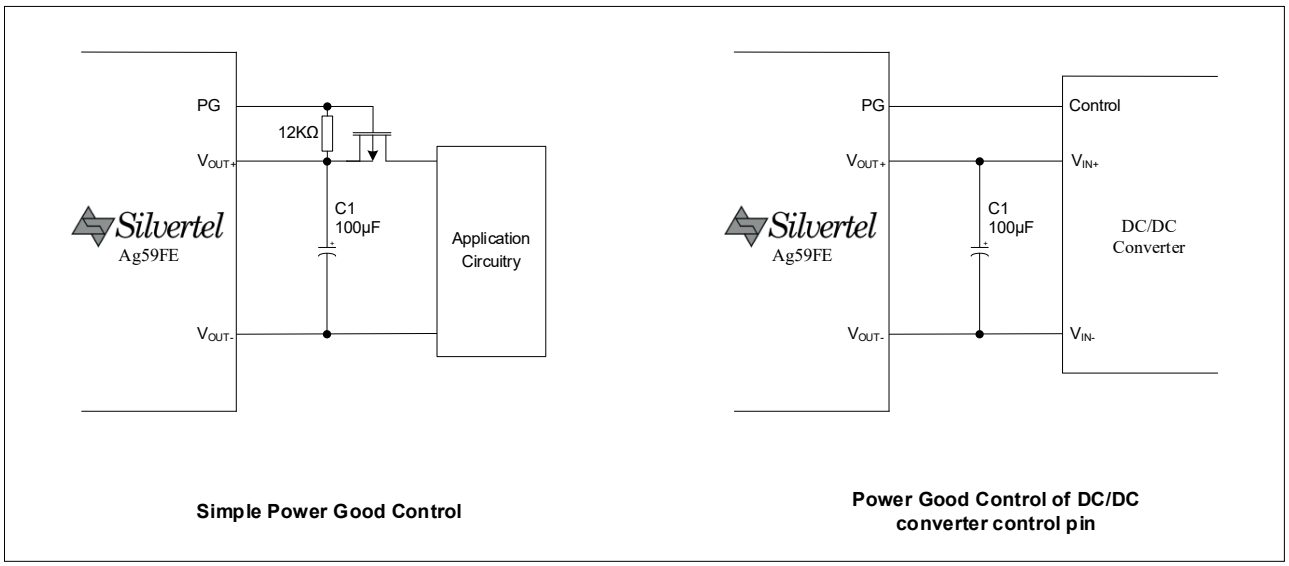


Figure 7: Inrush Control

4 Operating Temperature Range

The Ag59FE consumes very little power in normal operation, there are no specific requirements for thermal management for operation up to a maximum of 85˚C ambient, and a minimum of -40˚C ambient.

5 Isolation

To meet the safety isolation requirements of IEEE802.3 specification, a powered device must provide electrical isolation between all its accessible external connectors, including frame ground. In order to meet this requirement, the powered device should be subjected to and pass at least one of the following electrical strength tests of IEC 60950-1:2001 sub clause 6.2.1.

a) 1500V_{rms} at 50-60Hz for 60 seconds

b) 2250V_{dc} for 60 seconds or

c) 1500V_{dc} impulse test 10 times in either polarity.

The Ag59FE does not provide any isolation between its inputs or outputs, this should be implemented by use of an isolating DC/DC converter or isolated enclosure in order to meet the isolation requirement, see “ANX-POE-Isolation-Barrier” for more details.

6 Power Dissipation

The Ag59FE has been designed to dissipate as little power as possible. The following graphs show the typical power dissipation that can be obtained relative to the Line Voltage supplied at the input of the module.

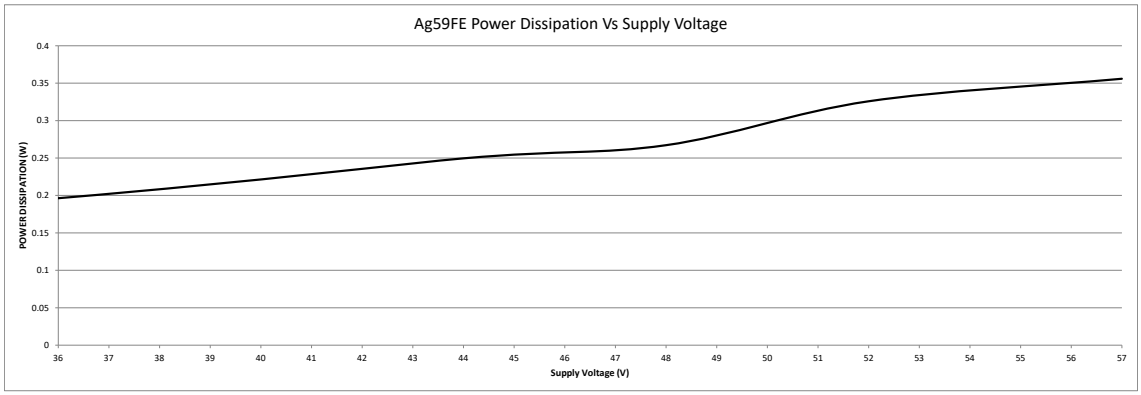


Figure 8: Ag59FE Power Dissipation

7 EMC

The Ag59FE has been designed to pass EN55032 Class B, however the Ag59FE will only be one component within the system so we would always advise that provisions are put in place in case further noise reductions are needed. Due to the requirements in PoE detection there are limitations on filtering circuitry positioned between the Ag59FE and the cable. As a result, it is recommended that the common mode filtering for the application is positioned on the output of the module.

8 Protection

8.1 Input Protection

The Ag59FE may be damaged by input voltage transients greater than 80V. For protection against electrostatic discharge (ESD) or other high voltage transients an over-voltage clamping device such as a 58V TVS Diode can be fitted across the V_{IN+} and V_{IN-} input pins, see Figure 9 and Apps Note “ANX-POE-Protection” for more details.

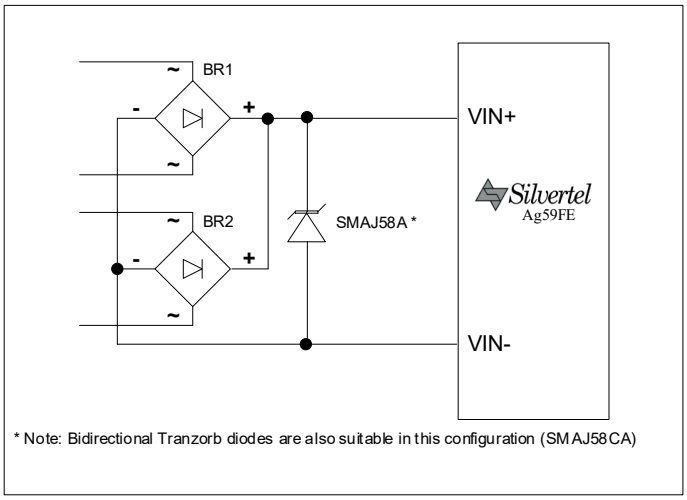


Figure 9: Input Protection

8.2 Output Back Feed Protection

While the Ag59FE will not be damaged from an auxiliary supply voltage to the output while PoE is not operating. The auxiliary supply voltage will back feed through the module and be present the input of the Ag59FE. This will result in the module being incapable of negotiating power if connected to a PSE. The voltage will not pass onto the ethernet port as it will be blocked from the cable by the input rectifiers.

If PoE is intended to provide redundant power in combination with an external or auxiliary supply, it is essential that a blocking diode or gating circuitry is implemented to prevent voltage injection on to the output of the module.

8.3 Thermal Protection

The Ag59FE dissipates very little power, as such it does not require or contain any built in thermal protection.

9 Solderability

The Ag59FE has been designed to be compatible with various assembly methods in mind. The part can be horizontally mounted for a low profile fully automated assembly process, the part can be vertically mounted using a routed slot with slot edge aligned pads or use with wave or manual assembly processes.

The module is lead-free (Pb-free) and RoHS compliant and fully compatible with a Pb-free automated assembly process. The Ag59FE can still be mounted manually using soldering iron or hot air.

There are no specific requirements regarding stencil thickness or solder paste classification type. For horizontal mounting, Non-solder mask defined (NSMD) pads are preferred over solder mask defined (SMD) pads, the land pattern dimensions are given in Figure 11: Land Pattern.

The Ag59FE contains no components of greater than Moisture Sensitivity level 1, as a result no special processes are required in the reflowing process of the Ag59FE.

Note : Do not pass the Ag59FE through the reflow process mounted to the underside of the assembly due to the risk of components falling off the module.

9.1 Solder Profile

Below is a typical profile that can be used to mount the Ag59FE in a vertical orientation, based on the J-STD-020 standard for Pb-Free applications. Exceeding these specifications may cause damage to the module. All production environments are different therefore please review these guidelines with the process engineer prior to use.

	Zone 1	Zone 2	Zone 3	Zone 4	Zone 5	Units
Zone Duration	42	42	42	42	42	Seconds
Top Heater	150	180	210	240	270	˚C
Bottom Heater	150	180	210	240	270	˚C
Typical Slope	2.1	1.2	1.1	0.9	0.8	˚C/Second
Airflow rate	40					M^3/Minute

Table 6: Solder Profile

	Min	Max	Units
Soak Time (s) 150-180˚C	30	90	Seconds
Time above (s) ≥217˚C	30	90	Seconds
Time within 5˚C of peak Temperature		30	Seconds
Target Peak Temperature (˚C)	230	245	˚C
ΔTemperature (˚C/s)	-6	3	˚C/Second

Table 7: Solder Parameters

10 Packaging

The default standard packing for the Ag59FE series is supplied in trays of 77.

11 Electrical Characteristics

11.1 Absolute Maximum Ratings

	Parameter[1]	Symbol	Min	Max	Units
1	DC Supply Voltage	V_{CC}	-0.3	60	V
2	Storage Temperature	T_S	-40	+100	°C
3	Moisture Sensitivity Level	MSL	-	1	-
4	Voltage MPS_Dis[2]		-0.3	3.1	V

Note 1: Exceeding the above ratings may cause permanent damage to the product. Functional operation under these conditions is not guaranteed. Maximum ratings assume free airflow.

Note 2: Voltage should not be injected into this pin. If unused leave floating, else pull to down to V_{in-}

11.2 Recommended Operating Conditions

	Parameter	Symbol	Min	Typ	Max	Units
1	Input Supply Voltage	V_{IN}	41	50	57	V
2	V_{out} enabled Voltage Threshold	V_{ULOCK}		32.5		V
3	V_{out} enabled Hysteresis	$V_{ULOCK-Hys}$		1		V
4	PG enabled Voltage Threshold	V_{PG}		38.2		V
5	PG enabled Hysteresis	V_{PG-Hys}		5.5		V
6	Operating Temperature	T_{OP}	-40	25	85	Ta / °C
7	Output capacitance[1]	C_{out}	0		180	µF
8	Output Load to meet MPS Requirement	I_{OUT_MPS}	7			mA

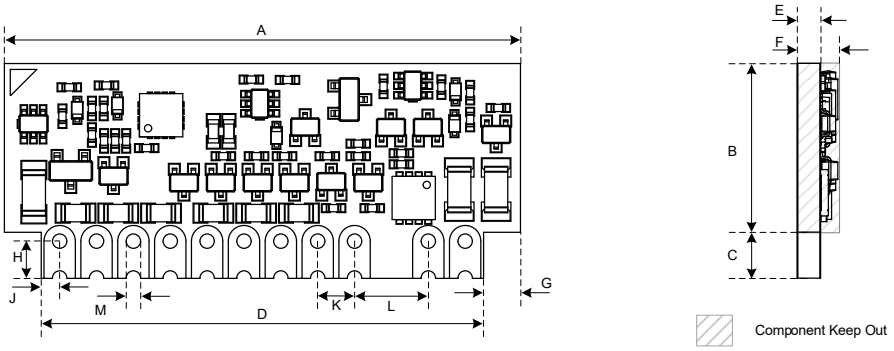
Note 1: Can be exceeded if inrush currents are limited.

11.3 DC Electrical Characteristics

	DC Characteristic	Sym	Min	Typ	Max	Units	Comments
1	Continuous Current output[2]	I_{LOAD}		1.68	2	A	@ 57V_{in}
2	MPS_DIS Logic Low	$V_{MPS\_DIS\_LOW}$	0	0.7		V	
3	DIS Logic Low	V_{DIS_LOW}	0	0.7		V	
4	Classification resistor Current	I_{Class}			50	mA	
5	TYP2_DET Current	I_{TYP2_DET}			2.2	mA	
6	TYP3_DET Current	I_{TYP3_DET}			2.2	mA	
7	PG Current	I_{PG}			2.2	mA	

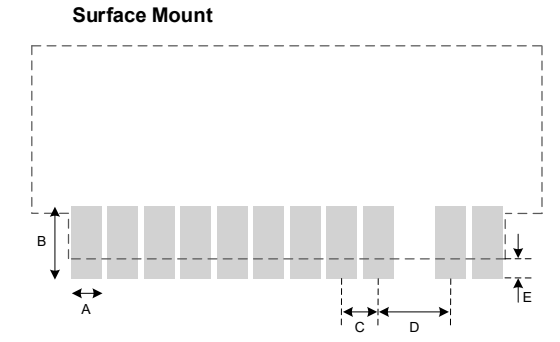
Note 1: Minimum 44V_{in} for maximum output at 25˚C. Maximum output power may be limited by PSE.

12 Package



Dimension	Millimetres		Inches	
	Nominal	Max	Nominal	Max
A	35.56	36.56	1.400	1.439
B	11.63	12.23	0.458	0.482
C	3.18	3.28	0.125	0.129
D	30.48	30.68	1.200	1.208
E	1.60	1.76	0.063	0.069
F	2.70	3.06	0.106	0.120
G	2.54	2.74	0.100	0.108
H	2.57	2.67	0.101	0.105
J	2.59	2.69	0.102	0.106
K	2.54	2.64	0.100	0.104
L	5.08	5.18	0.200	0.204
M	0.94	1.02	0.037	0.040

Figure 10: Package Dimensions



Dimension	Millimetres	Inches
A	2.13	0.084
B	5.08	0.200
C	2.54	0.100
D	5.08	0.200
E	1.45	0.057
f	1.78	0.070
g	2.03	0.080
h	1.80	0.071
j	30.99	1.220

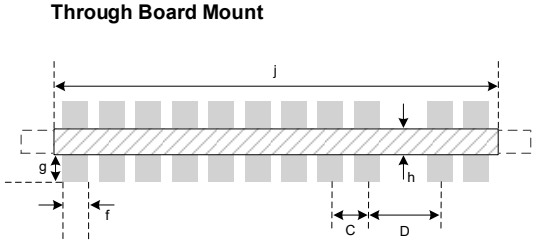


Figure 11: Land Pattern