ANX-POE-Power

Available power over PoE

Introduction

There is a common misconception regarding the power available to a device with Power over Ethernet (PoE) over the advertised power available for each standard. This application note is created as a guide to help understand the power available, and where power can be lost in a PoE application, in order to assist in adhering to the correct power limits when implementing a Silvertel module into an application such that (classification) power limits are not being exceeded.

PoE Power Limits Overview

There have been three amendments to the IEEE802.3 specification regarding PoE, covering low power applications all the way up to applications with 90W of power usage. The first amendment to the specification was IEEE802.3af, this introduced Type 1 devices, which allowed for applications drawing up to 15.4W, with the IEEE802.3at amendment adding Type 2 devices for up to 30W of power, and finally the IEEE802.3bt added Type 3 and Type 4 devices for up to 90W applications.

There are three elements to a PoE application, the Power Sourcing Equipment (PSE), Physical interface (PI) and the Powered Device (PD). The PSE is typically a switch or injector that supplies the DC power to the Ethernet cable alongside the data. The PI is the Ethernet cable that connects the PSE to the PD.

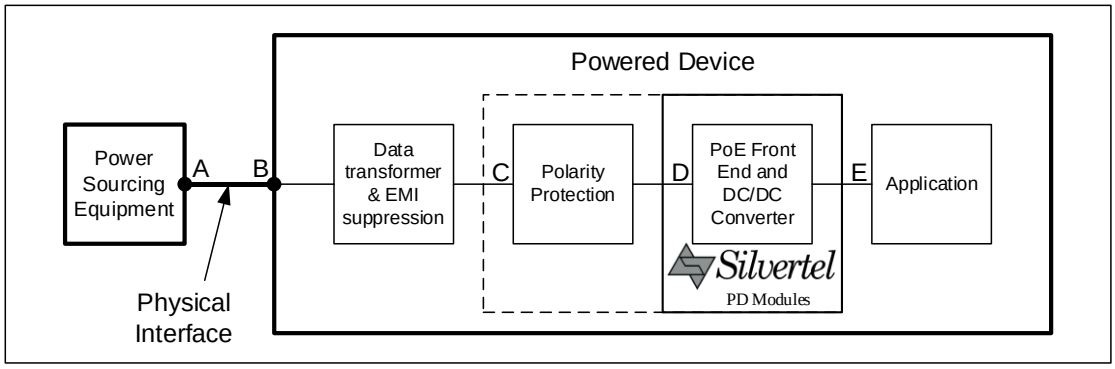

Figure 1: PoE Overview

It is important to note that the power figures stated above are not the power available to the PD application. They are the minimum amount of power the PSE should supply over any voltage measured at point A in Figure 1. This is typically the RJ45 connector of the switch or injector, and does not account for the power losses involved in transmission.

Device Type	Minimum PSE output power Point A (W)	maximum loop resistance (Ω)	Requested Class	Minimum power availible to PD Point B (W)
1	15.4	20	0	12.95
	4	20	1	3.84
	7	20	2	6.49
	15.4	20	3	12.95
2	30	12.5	4	25.5
3	45	12.5	5	40
	60	12.5	6	51
4	75	12.5	7	62
	90	12.5	8	71.3

Table 1: Available Power

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Table 1 shows the guaranteed power available for each requested class at Point B in Figure 1, which is normally the RJ45 connector to the designed application device. This power available is calculated by using the minimum continuous supply voltage allowed for a PSE, of the given Type, over 100m of cable with the worst loop resistance allowable by the specification. In a real world situation, there will be more power available to the PD, as the cable resistance will be lower, the PSE may be outputting a higher voltage and the PSE may allow for a greater than minimum power to be drawn consistently. It is strongly recommended for reliable operation that any device being designed should only draw up to this guaranteed available power for any given class.

What follows is an explanation of each stage where power can be lost in a PoE application and some general principles for reducing loss.

Transmission Losses

In the first iteration of PoE, the cabling was rated to have a maximum pairset resistance of 20Ω for 100 metres of cable, this is the combined resistance for pairs 1-2 in series with pairs 3-6 (or 4-5 and 7-8 for Alt B operation). The maximum DC current in a type 1 system is 350mA; as a result up to 0.350^2 x 20 = 2.45W can be lost in the cable. This is where the 12.95W minimum available power for a class 3 device from Table 1 is calculated 15.4 - 2.45 = 12.95W.

With the announcement of Type 2 devices in the IEEE802.3at amendment, the maximum cable loop resistance was reduced to 12.5Ω. This reduces losses and adds a new higher maximum current of 600mA down a pairset.

Type 3 power systems, as detailed in amendment IEEE802.3bt, follow the same specifications as Type 2 devices but require the power be delivered over both pairsets (8 conductors), with class 6 devices able to draw up to 600mA on each pairset. For Type 4 devices, the maximum continuous current per pairset is increased up to 900mA for class 8 devices.

Requested Class	Transmission losses (W)
0	≤2.45
1	≤0.16
2	≤0.51
3	≤2.45
4	≤4.5
5	≤5.0
6	≤9.0
7	≤13.0
8	≤18.7

Table 2: Transmission loss

While the losses in transmission can be significant, and often not as extreme as those stated in Table 2, they are normally outside the control of the product manufacturer and as such, it is good practice to design the power envelop of a product to be within the figures above. If the manufacturer can specify the PSE used or the length and quality of cabling, then the minimum power level for the PD application can be increased according to the improved specifications.

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Polarity protection

PDs are required to be insensitive to the polarity of the power supplied over each pairset, as a result rectification is required. This rectification can be the source of a large amount of power loss in a PoE system, especially with higher power applications. In general there are three technologies when it comes to rectification, standard diode arrays, Schottky diode arrays featuring a reduced voltage drop, and ideal rectification using MOSFETs to virtually eliminate the voltage drop in rectification.

To highlight the differences in technology a Silvertel Ag5412 PD Module was fitted to an EvalAgSil evaluation board and then tested with the three supplied different bridge rectifier modules and additionally a shorted bridge rectifier module created to be used as a comparison. Figure 2 shows the power dissipation of the bridge rectifiers by removing the power usage of the shorted bridge rectifier results from each of the bridge rectifier results.

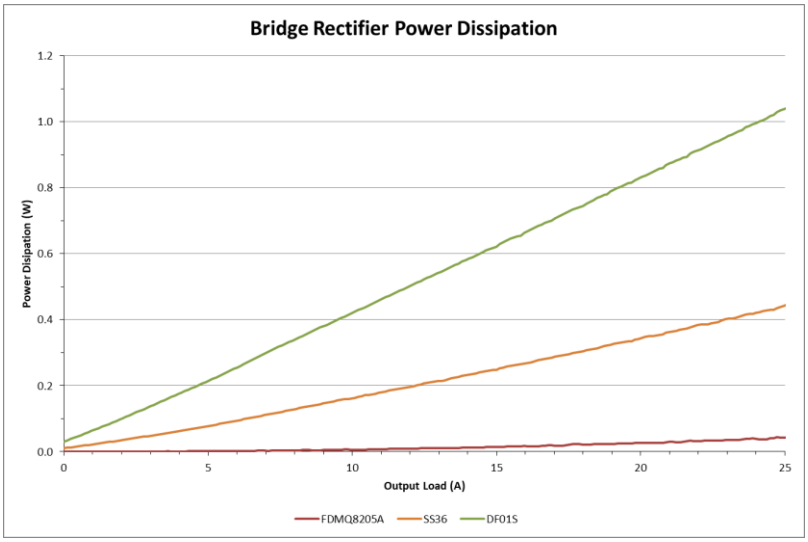

Figure 2: Bridge rectifier dissipation

The first bridge rectifier module utilises the DF01S which is a standard diode bridge rectifier with a forward voltage drop of approximately 0.9V per element. This is the cheapest option but will incur the most losses out of any rectification technology. This type of rectification is not recommended in Type 3 or 4 applications due to the significant losses and heat dissipation associated with the higher supply current.

The Second bridge rectifier module utilises the lower voltage drop of Schottky barrier rectifiers in the form of 8x SS36 diodes. These feature a lower forward voltage drop of less than 0.4V, resulting in a significant drop in losses in comparison to the DF01S module.

The final bridge rectifier module utilises active MOSFET rectification by using two FDMQ8205A ICs. This is the most expensive option, but offers the best performance in terms of losses. These provide a typical series resistance of 130mΩ on each pairset while power is supplied to the device, there will also be a small loss due to the internal drive circuitry.

The Ag5412 PD Module can achieve an efficiency of 93.3% under normal conditions, but can only achieve 92.4% in this evaluation board setup; the additional loss will be due to the resistance of the traces and the sockets for the bridge rectifier module and the Ag5412 module. Table 3 shows the maximum output power that can be achieved before the 25.5W input power is reached.

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Bridge Rectifier fitted	Max power Output (W)	Difference (W)
Ag5412 only	23.45	
FDMQ8205A	23.34	-0.11
'SS36	23.21	-0.24
DF01S	22.74	-0.71

Table 3: Maximum Output Power

EMI Suppression

When it comes to EMI suppression, the recommended circuit Silvertel recommends is three 1kΩ @100MHz ferrite beads on both the V_{in+} and V_{in-} rails. This is a general purpose recommendation that should provide more than adequate suppression for the vast majority of applications. This comes with the trade-off of efficiency, adding more than the required amount of suppression to a circuit reduces its efficiency and adds more heat to dissipate inside the enclosure.

Even if a given level of suppression is required in an application, there are methods of reducing the losses. As standard, fitted to the EvalAgSil, are six Wurth 742792096 1kΩ @100MHz ferrite beads, these are rated for up to 1A with DC resistance of less than 0.3Ω in an 0805 package, however this equates to almost 1.8Ω resistance on a rail supplying up to 1.8A for a class 8 device.

One method of reducing these losses is to increase the package size of the ferrite beads. As an example six Taiyo Yuden FBMH4525HM102NT ferrite beads were installed, these are still rated at 1kΩ @100MHz but are rated for up to 3A in an 1810 package and have DC resistance of less than 0.06Ω. This has a significant saving in power dissipation as can be seen in Figure 3, at the expense of a much larger board area required to fit the larger components.

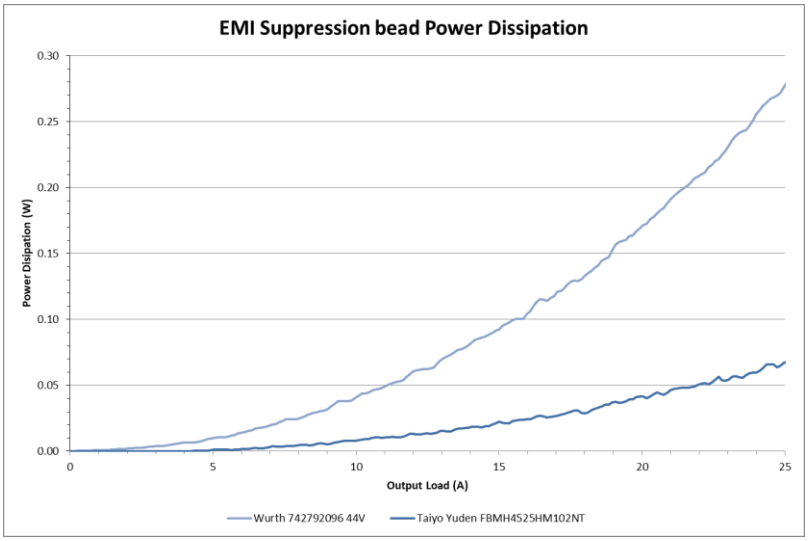

Figure 3: Ferrite bead dissipation

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Data Transformer

The power dissipated across the Ethernet data transformer is small relative to the power delivered to the application but it is still a source of power loss. Fitted to the majority of Silvertel's evaluation boards including the EvalAgSil is the Wurth 749052050. As a comparison an Abracon ALAN310001-3J61DT transformer was fitted to the EvalAgSil. While both of these transformers are rated for up to 100W applications, the Wurth part is a more premium option, which as a result features lower DC resistance for similar levels of performance, this can be seen in Figure 4 with the Wurth data transformer dissipating less than half of the power of the Abracon transformer at 25W.

For high power applications, it should be noted that this extra dissipation may result in a significant difference in temperature between the two transformers tested.

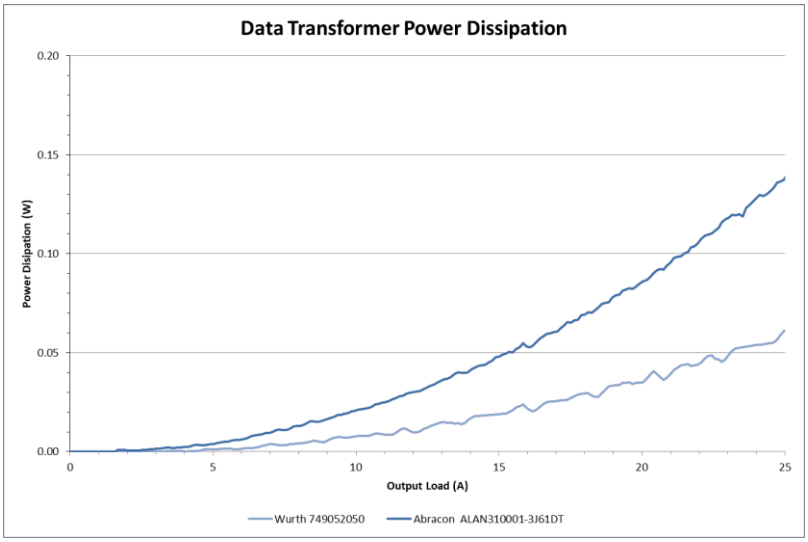

Figure 4: Data transformer dissipation

Trace Length

The final element that should be considered for power losses is the traces in the board itself. For a standard 1oz copper PCB layer, a 10mil track will have a resistance of approximately 0.05Ω for every inch of track. Since these tracks are in series with each other, it can be assumed that there is 0.1Ω of resistance added for every inch the traces have to be routed to connect the Rj45 connector to the module's pins.

As a result it is recommended to fit the data transformer as close as possible to the RJ45, and fit the module close to the data transformer with as wide tracks as possible in a design avoiding vias and right angles were possible, as these will increase the resistance of the trace.

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Example

Here is an example of where power losses can occur in a typical setup: an EvalAg6800 PSE supplied with 56V connected to an EvalAg5800 PD set to output 6.5A at 12V via a 0.5 metre patch cable. The losses in this example are only indicative of an actual setup as the evaluation boards contain unnecessary circuitry, sockets and longer than necessary tracks in order to help facilitate evaluation of the fitted modules.

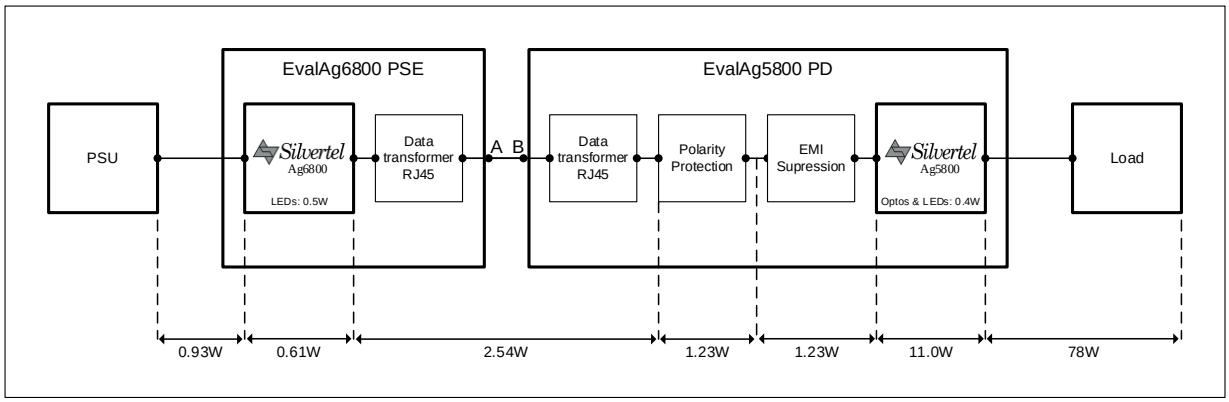

Figure 5: Example Setup

- Between the PSU and the V_{IN} pins on the Ag6800 there is 0.93W loss. This is due to the cabling, connector and sockets on the module.
- In the Ag6800 there is 0.61W consumed; 0.5W of this is the power and status LEDs on the EvalAg6800.
- Between the Ag6800 and the input to the bridge rectifiers there is 2.54W loss. This is lost in the cabling, RJ45 connectors and module sockets, the resistance of the two data transformers, and the traces on the evaluation boards.
- Across the Schottky bridge rectifiers 1.23W is lost with a further 1.23W across the ferrites used for EMI suppression.
- The power draw of the Ag5800 for a 6.5A output and 52V supply is 10.6W. The measured supply voltage to the Ag5800 is 52.53V due to all the losses before the module. Added to this status LEDs and opto-coupler on the EvalAg5800 consume 0.4W.

As you can see the losses in the evaluation board setup above are approximately 17.5W, meaning that in order to supply 78W of power to the load, there is approximately 94W output from the Ag6800, with a total of 95.5W drawn from the PSU.

It is important to note that these are not fixed losses. In a designed system any losses due to the Ag6800 module sockets and the long traces on the evaluation boards will be reduced, and for example the LEDs are not necessary, they could be reduced or removed.

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