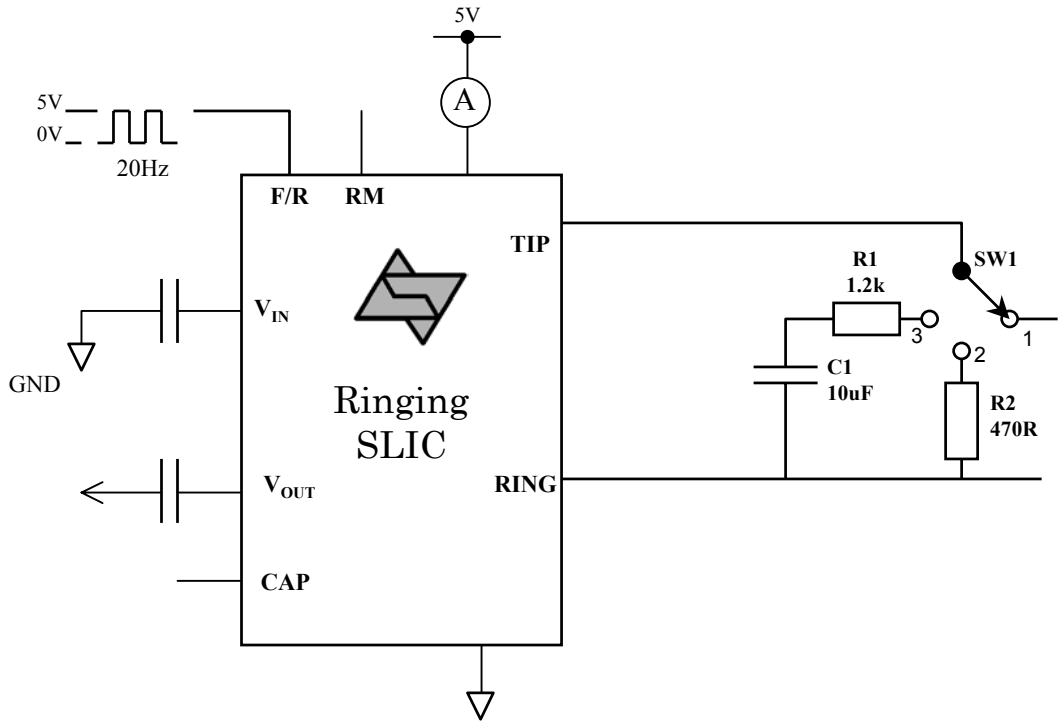
TEST CIRCUITS FOR SLIC INTERFACES

Silver Telecom Product Datasheets contain an Applications Diagram. This shows the electrical connections and typical values of external components required, when using our products.

Always consult the datasheet before performing parametric testing.

The basic parametric test circuits, used by Silver Telecom when testing SLIC Interfaces, are shown on the following pages.

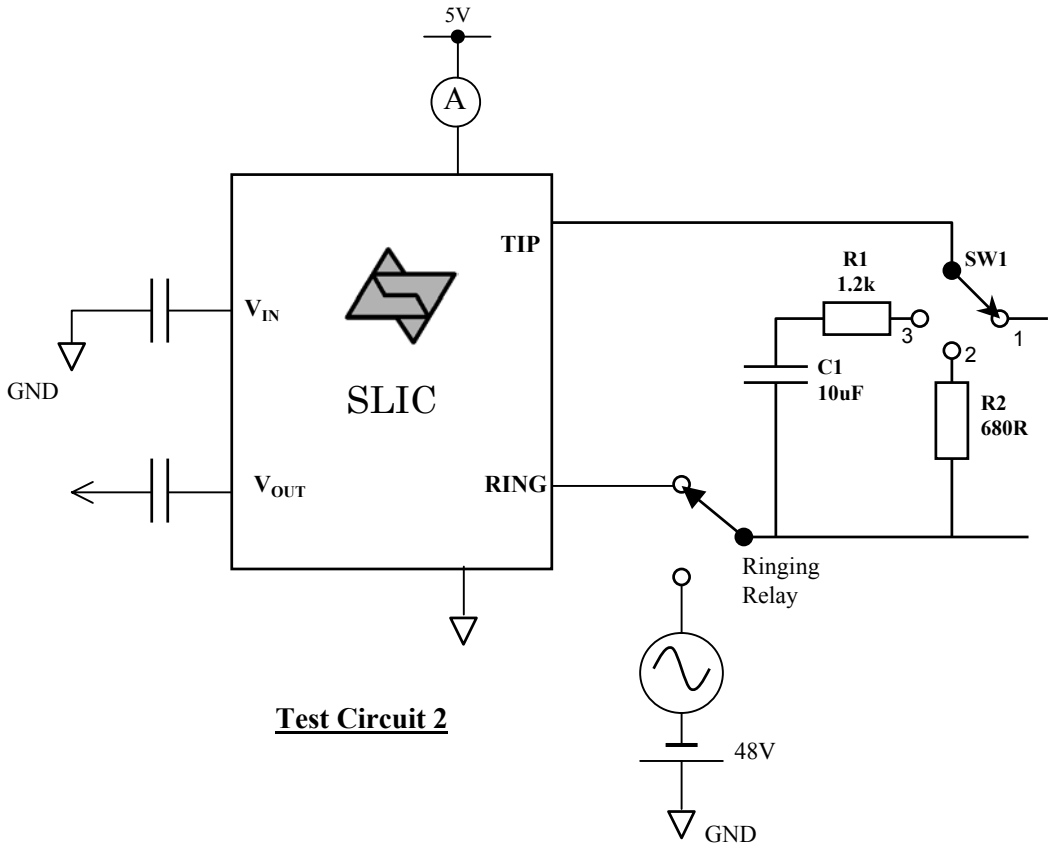
DC ELECTRICAL FOR RINGING SLIC



Test Circuit 1

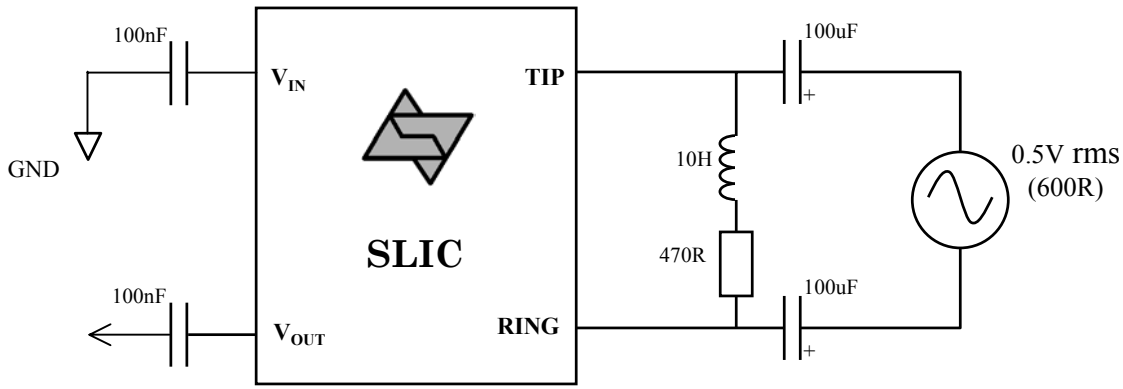
NOTE: Ag1160 and Ag1460 need a 220nF slew rate capacitor connected from CAP pins to Ground

DC ELECTRICAL FOR NON-RINGING SLIC



Test Circuit 2

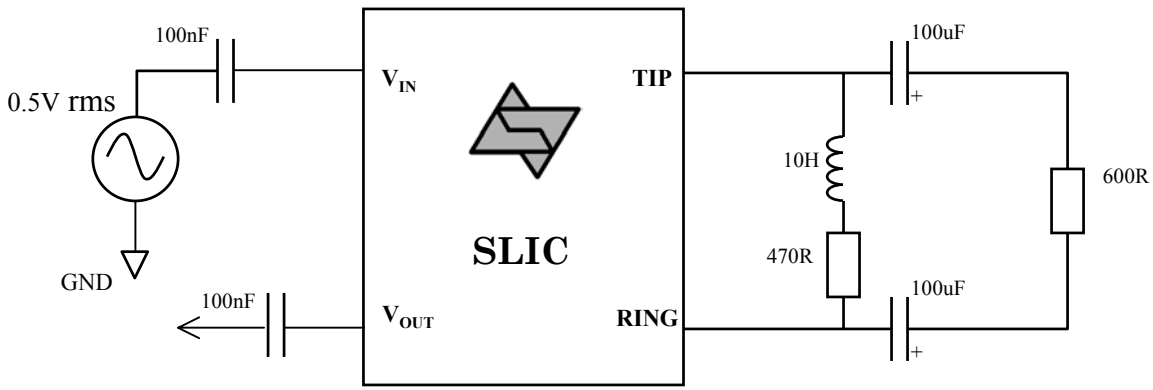
TRANSMIT GAIN TEST (2W TO VOUT)



Test Circuit 3

Transmit Gain = 20 log (V_{OUT} / V_{T-R})

RECEIVE GAIN TEST (VIN TO 2W)
TRANSHYBRID LOSS

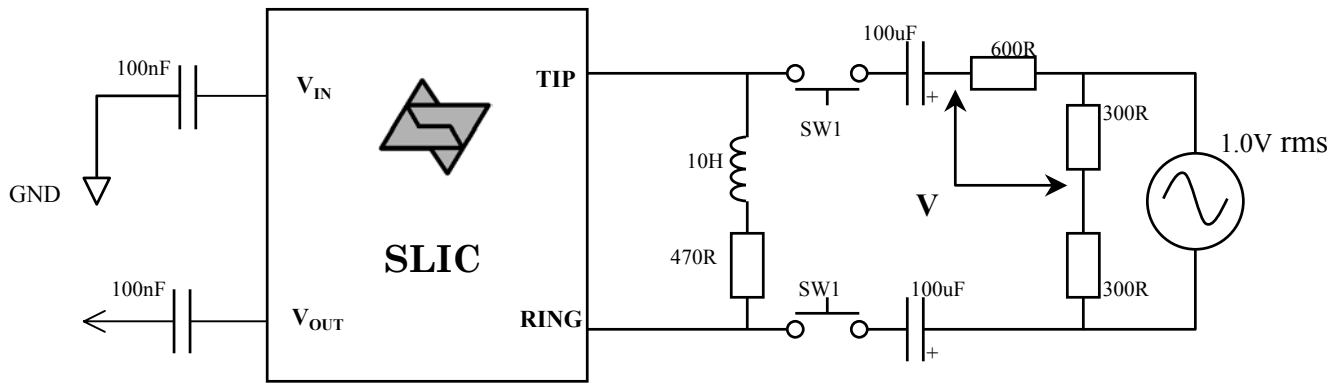


Test Circuit 4

Receive Gain = 20 log (V_{T-R} / V_{IN})

Trans Hybrid Loss = 20 log (V_{OUT} / V_{IN})

2-WIRE RETURN LOSS



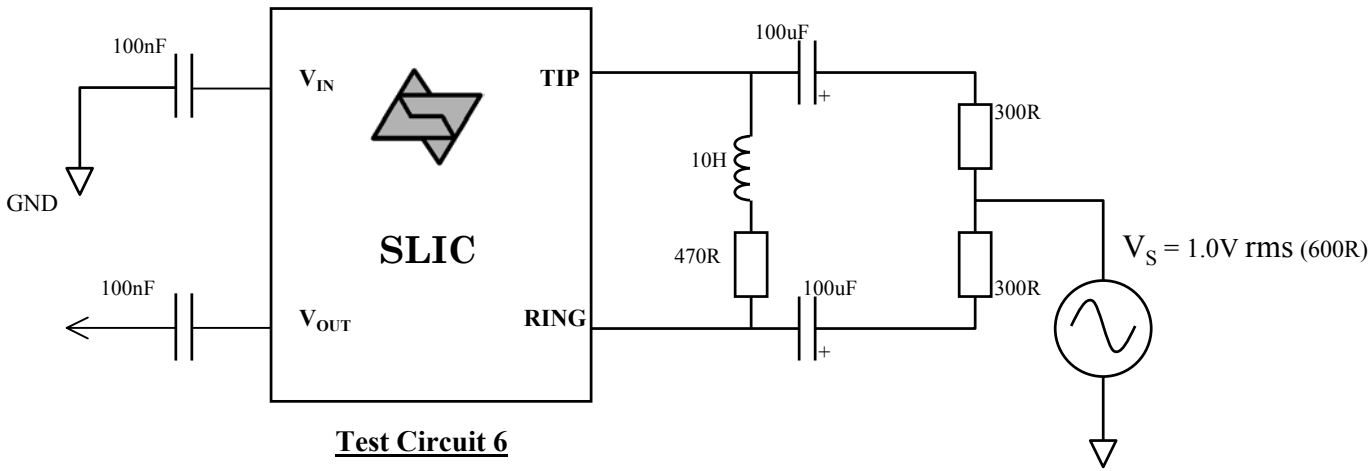
Test Circuit 5

2W Return Loss = 20 log (V1 / V2)

Where V1 = V with switch closed

and V2 = V with switch open

COMMON MODE REJECTION RATIO (CMRR)
LONGITUDINAL TO METALLIC BALANCE (LCL)

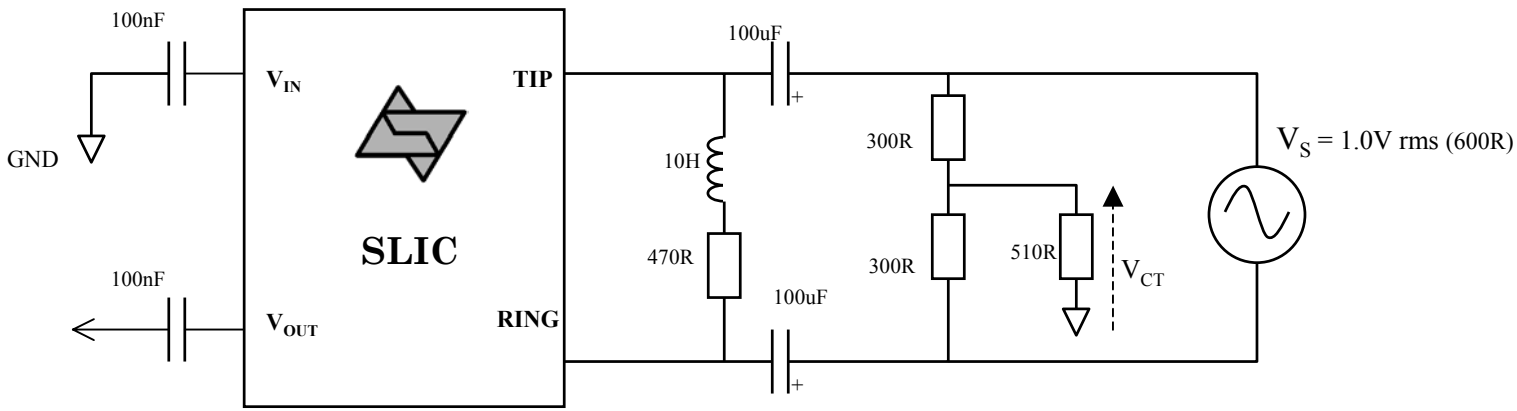


Test Circuit 6

$$CMRR = 20 \log (V_{OUT} / V_S)$$

$$\text{Longitudinal To Metallic Balance (LCL)} = 20 \log (V_{T\text{-}R} / V_S)$$

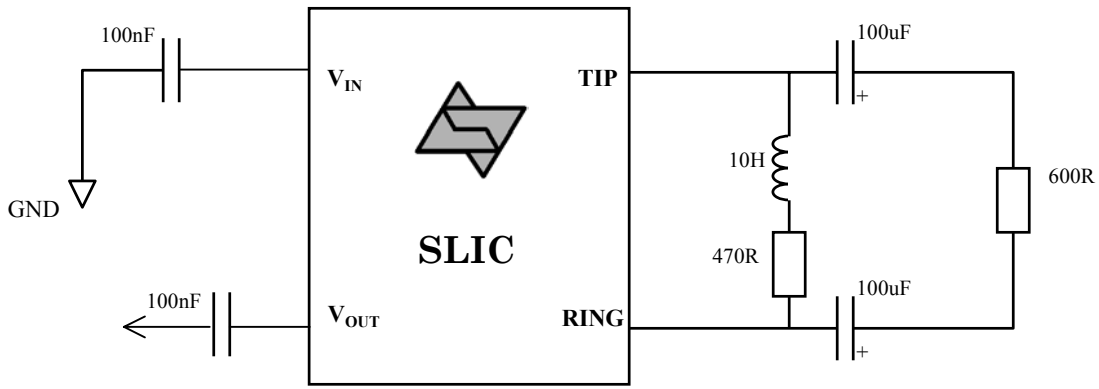
METALLIC TO LONGITUDINAL BALANCE (TCL)



Test Circuit 7

Metallic to Longitudinal Balance = 20 log (V_{CT} / V_{T-R})

CMESSAGE NOISE AT 4W AND 2W



Test Circuit 8

2W Noise = 20 log (V_{T-R} / 0.775) NOTE: Measure V_{T-R} with a Cmess filter and true RMS meter.

4W Noise = 20 log (V_{OUT} / 0.775) NOTE: Measure V_{OUT} with a Cmess filter and true RMS meter.