Ag5100 - Gating Output with an External Power Supply

This application note shows how to gate the Ag5100 output with an external power supply; that has priority over the Power over Ethernet (PoE) supply.

Parallel Configuration

With only the PoE input connected, the ADJ input of the Ag5100 is connected to OV1 via R1. This will increase the nominal output voltage at VOUT1 (and VOUT2) to ~ 12.5V. D4 is a Schottky diode with a forward voltage drop of ~ 0.5V, therefore the voltage supplied to the device will be ~ +12.0V.

If an external +12Vdc to 13Vdc supply is also connected, D1 will take the ADJ input high (limited by the zener diode D2), reducing the output voltage at VOUT1 to nominal ~ +9.8V. At the same time D3 will start to conduct maintaining the supply to the device at ~ +12.0V. The external supply will also turn Q1 ON via R3, this will connect the load resistor R4 across the Ag5100 output to ensure the part drive its minimum load.

If the external supply is removed the ADJ input will go low again, VOUT1 will return to ~ +12.5V and the Ag5100 will resume supplying power to the device via D4. Q1 will turn OFF and the load resistor R4 will be removed.

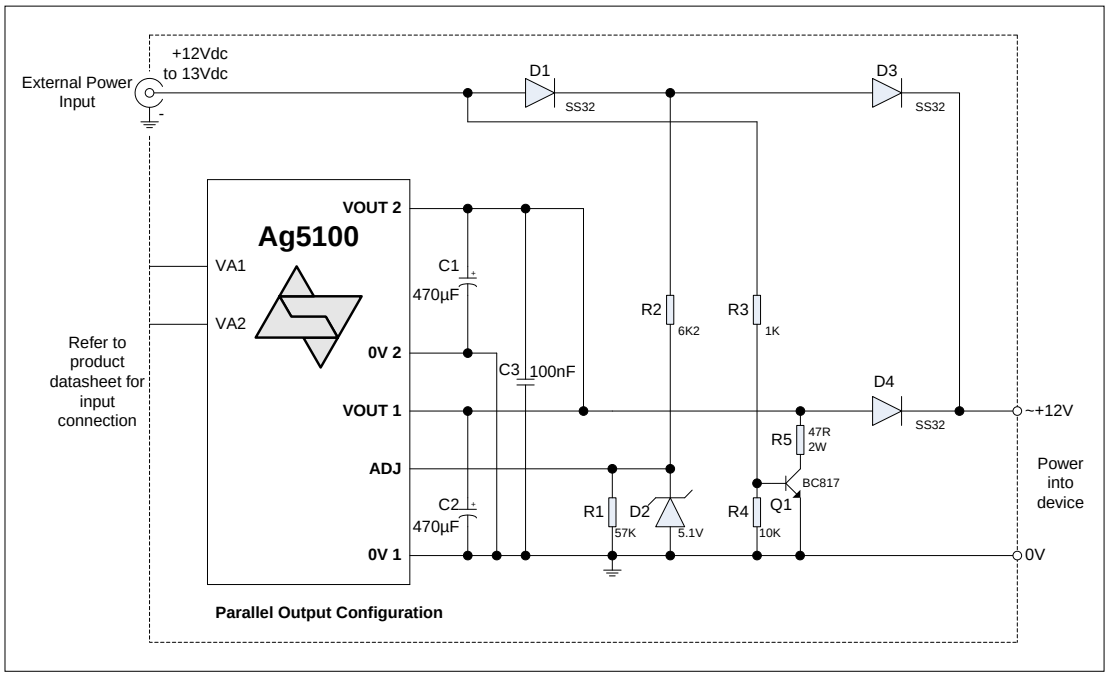

Figure 1: Parallel Output Configuration

Series Configuration 1

With only the PoE input connected, the ADJ input of the Ag5100 is connected to OV1 via R1. This will increase the nominal output voltage at VOUT2 to ~ 24.5V. D4 is a Schottky diode with a forward voltage drop of ~ 0.5V, therefore the voltage supplied to the device will be ~ +24.0V.

If an external +24Vdc to 26Vdc supply is also connected, D1 will take the ADJ input high (limited by the zener diode D2), reducing the output voltage at VOUT2 to nominal ~ +19.3V. At the same time D3 will start to conduct maintaining the supply to the device at ~ +24.0V. The external supply will also turn Q1 ON via R3, this will connect the load resistor R4 across the Ag5100 output to ensure the part drive its minimum load.

If the external supply is removed the ADJ input will go low again, VOUT2 will return to ~ +24.5V and the Ag5100 will resume supplying power to the device via D4. Q1 will turn OFF and the load resistor R4 will be removed.

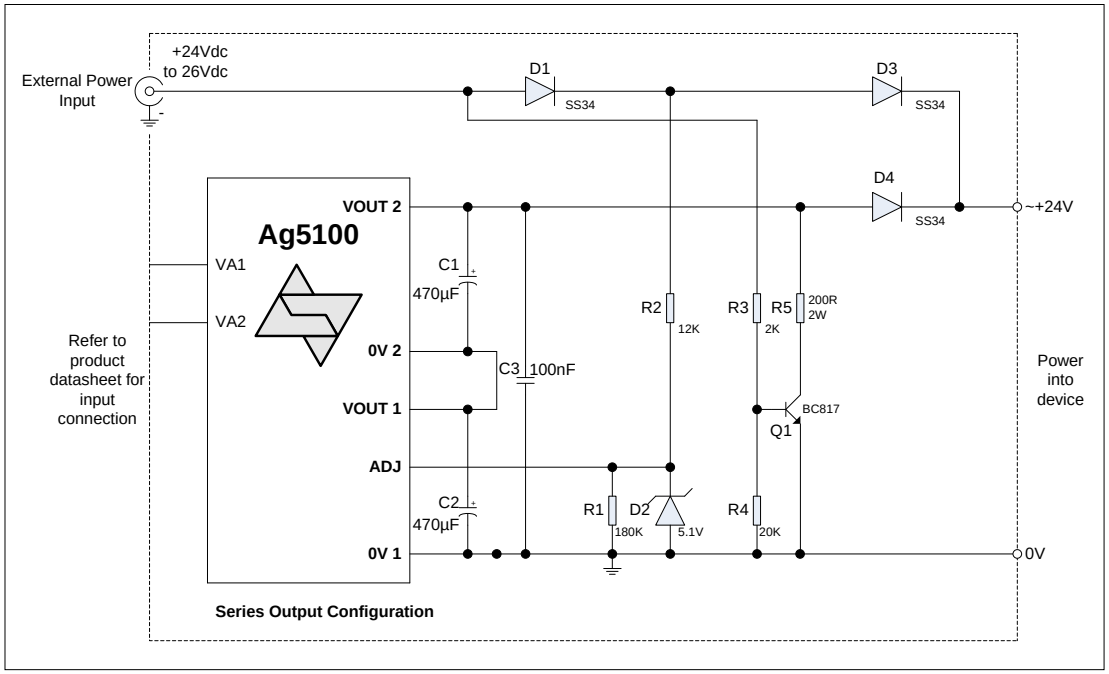

Figure 2: Series Output Configuration

Note: In both output configurations it is important that C1, C2 and C3 are positioned as close to output pins as possible. See the Ag5100 Output Configuration application note (AN5100-1) for further details.