Ag1170 Simple Power Down Circuit

The Ag1170 has a PD pin, which can be used to power down the module to reduce the operating supply current when the system is in idle (stand-by) mode. Normally this would be connected to a controller (via a transistor), but in cases where the controller is also shut down this may not be practical.

This application note shows a simple method (Figure 1) of using a CMOS 555 Timer to put the Ag1170 into power down, waking the module up once a second to test the status on the phone.

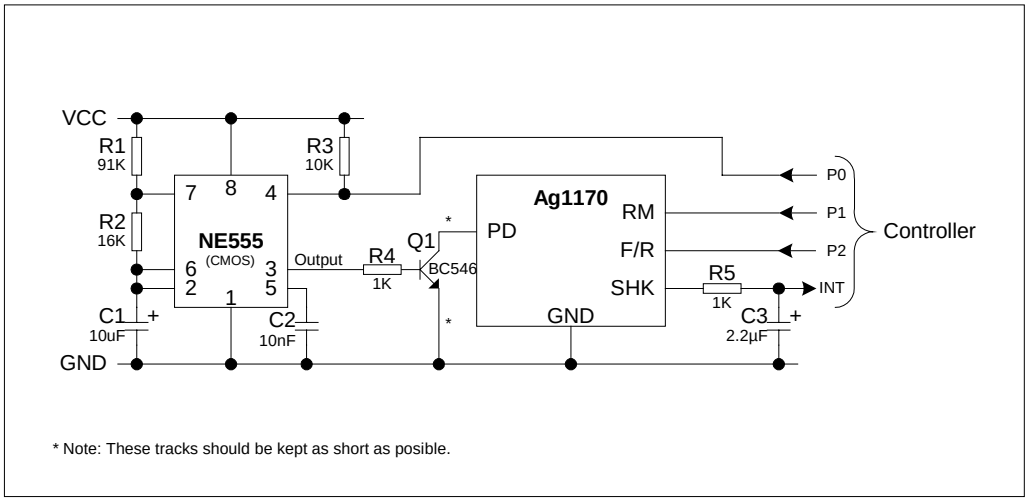

Figure 1: Power Down Circuit

Operation

During normal operation the Controller must set P0 low which resets the Timer. When the Timer is held in reset its Output pin is set low, this switches Q1 OFF, allowing the Ag1170 DC/DC converter to operate normally.

To put the Ag1170 into power down mode the controller must set P0 high, this removes the reset from the timer allowing it to go into astable operation. During astable operation R1, R2 and C1 set the duty cycle to ~1000ms (~1Hz), with a 9:1 mark – space ratio.

When the Timer Output pin goes high, Q1 will switch ON and PD will go low disabling the Ag1170 DC/DC converter.

When Timer Output pin goes low, the Ag1170 will wake-up so that the SHK pin can be monitored to see if the phone has gone OFF-Hook. During wake-up the SHK output will go high for up to 25ms, R5 and C3 have been added to stop this pulse from activating the controller interrupt. If the phone is OFF-Hook the SHK output will stay high for mark duration (~100ms), which will be long enough for the INT pin to go high (activating the interrupt).

When an interrupt is detected the controller must set the P0 output low restoring the Ag1170 back to normal operation.

This circuit reduces the average operating current of the Ag1170 from ~100mA in Normal mode (P0 low), to ~10mA in idle mode (P0 high).