POE Ag5510 Evaluation Board User Manual

Rev 1.0 – August 2016

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3 Introduction

This manual is intended to be a guide to using the “EVALAg5510” (Rev 1R or higher) evaluation board with an Ag5510 Powered Device (PD) module.

The EVALAg5510 evaluation board should be powered using both the spare pair (pins 4&5 and pins 7&8) and the data pair (pins 1&2 and pins 3&6) in the CAT5e cable through the on-board magnetics.

4 Board Description

The input data and power is supplied to the board through connector J101. The data is passed through to the peripheral equipment via J100, with the output power from the Ag5510 module supplied via J3 to J5 (see Figure 1 & 4).

The EVALAg5510 on-board bridge rectifiers will ensure that the correct input polarity is applied to the Ag5510.

LED 1 indicates that power is being supplied to the Ag5510. This can be disabled by removing the jumper link LK1, removing these links does not affect the power being delivered to the Ag5510.

4.1 Input Signature and Classification

The EVALAg5510 board will automatically direct the power from J101 to the Ag5510’s input. LED1 will be illuminated when the PoE power is being applied to the board.

The Ag5510 provides a 26K signature required to be powered from an IEEE compliant PSE, however Phihong have developed a range of POE Ultra Power Sourcing Equipment (PSE) to provide higher power than specified in IEEE802.3at. The signature for this PSE range does not conform to the IEEE802.3af or IEEE802.3at standards, however the Ag5510 is designed to work with this range and LK7 will connect the SA1 and SA2 signature adjustment pins. For other PSEs ensure LK7 is not fitted.

The Ag5510 Classification is fixed at Class 4 but some high power PSE’s will only supply greater than IEEE802.3at limits if it recognizes Class 5. If Class 5 is required for the higher power PSE’s then LK5 should be fitted.

LED 6 will be illuminated, if LK4 is fitted, once the Ag5510 is powered and outputs 12V or 24V.

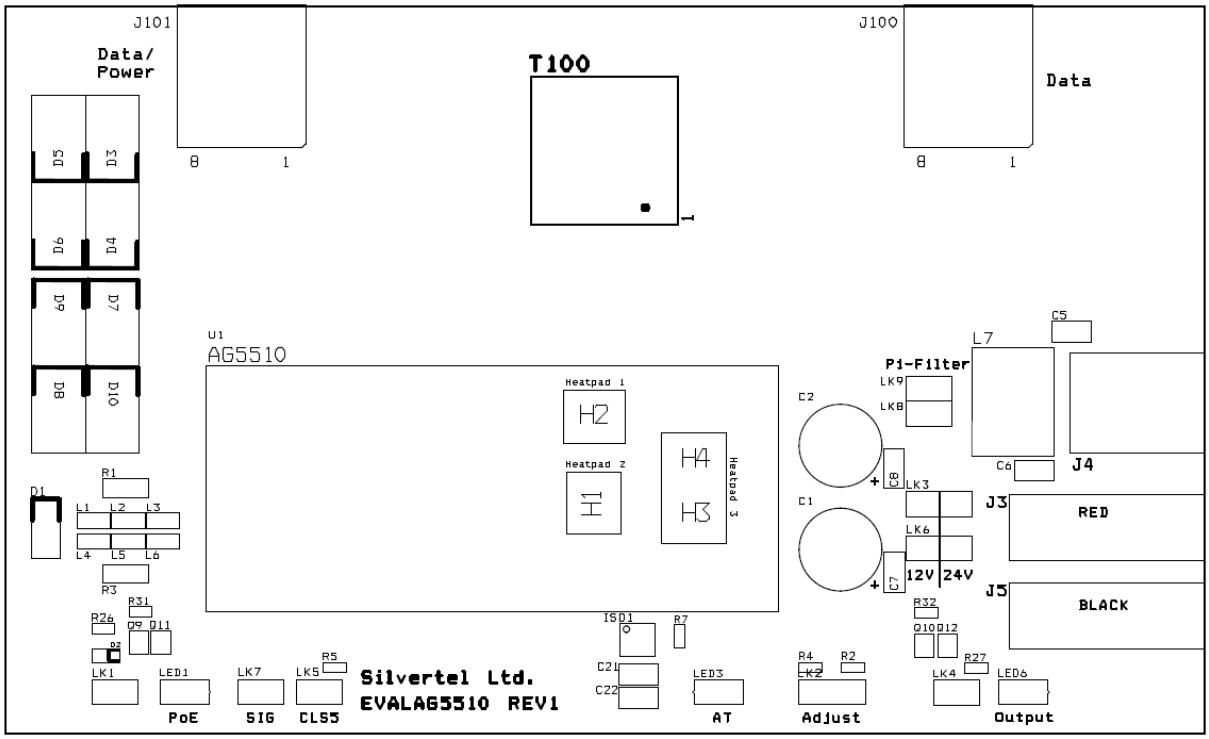

Figure 1: Board Layout

4.2 PD Output Selection

Before using the EVALAg5510 evaluation board, it is important to setup the output configuration jumpers for the correct output voltage.

The Ag5510 has two DC outputs that must be connected in parallel or in series. The outputs cannot be run independently so the EVALAg5510 board has output selector links LK3 and LK6. For parallel outputs both of these links must be in position “12V” - VOUT1 connected to VOUT 2 and 0V 1 connected to 0V 2. For series outputs both links must be in position “24V” – VOUT 1 connected to 0V 2. The DC10 connector J4 delivers a nominal 12V when the outputs are in parallel or 24V when the outputs are in series.

4.3 Output adjustment

The primary output (VOUT 1 – 0V 1) has an ADJ pin, which allows the output voltage to be increased or decreased from its nominal value. The secondary output (VOUT 2 – 0V 2) will track the adjusted primary output voltage.

The EVALAg5510 board has an adjust link LK2 and two resistors R2 (91K) and R4 (8K2) which allows the output to be adjusted to its maximum and minimum values.

To reduce the output voltage to its minimum level, connect a link to LK2 beneath R2. To increase the output voltage to its maximum level, connect a link beneath R4.

4.4 Output Filter

The Ag5510 output ripple and noise can be reduced by adding an additional output filter. By removing the links off LK8 & LK9 a Pi Filter will be placed in line with the output reducing the output ripple. By fitting the links the Pi Filter will be removed from the output, however the evaluation board does not show a true representation of the output ripple due to the resistive links and configurations fitted.

5 Typical Set-up

Figure 2 shows the basic set up using the EvalAg5510 evaluation board with a High Power Midspan or Endspan.

The equipment required: -

- Midspan or Endspan PSE (Power Sourcing Equipment)
- Peripheral (or Test) Equipment
- CAT5e cables
- Output power cable
- Mains cable

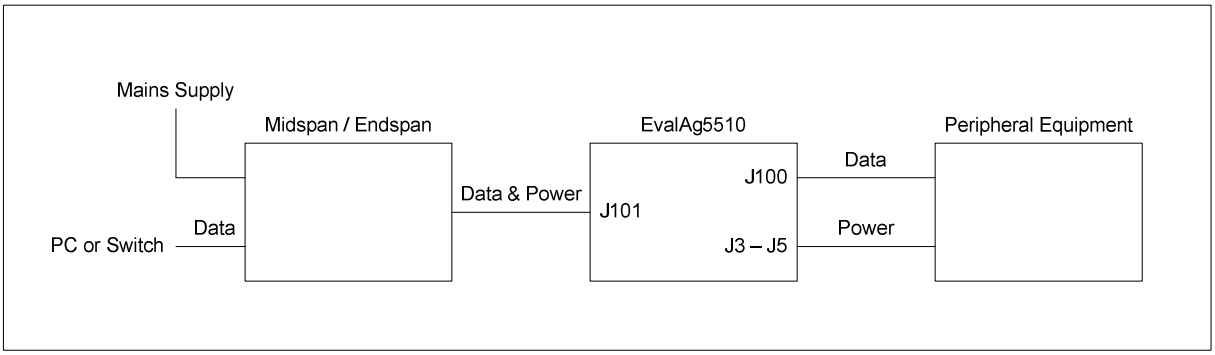

Figure 2: Basic set-up

6 Using the Board

6.1 Typical Application

Figure 3 shows an example set-up using an Ag5510 powered by a Phihong POE60U-560(G)-SS-R Midspan and supplying +12V to a Vivotek PZ6122 (or PZ6112) ethernet camera.

The PC ethernet port is connected to the data input of the POE60U-560(G)-SS-R (PSE) via a short Cat5e patch cable. The Data & Power output from the POE60U-560(G)-SS-R is connected to the input of the EVALAg5510 evaluation board (J101) via a CAT5e cable. The data output (J100) of the EVALAg5510 evaluation board is connected to the data port of the ethernet camera via a short CAT5e patch cable. The +12V (parallel configuration) power output from the EVALAg5510 evaluation board (J3-J5) connects to the dc input of the Vivotek PZ6122 ethernet camera.

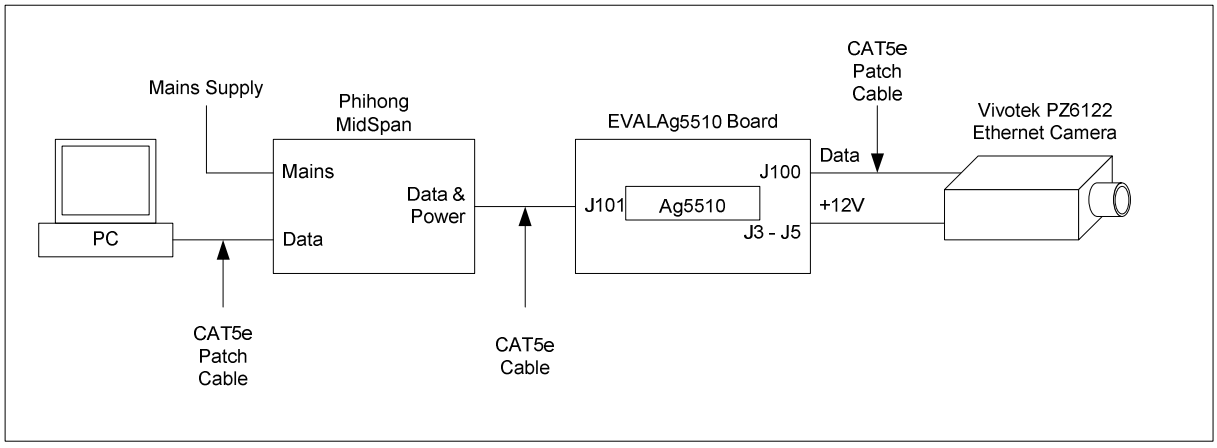

Figure 3: Example set-up

6.2 EVALAg5510 Evaluation Board Schematic

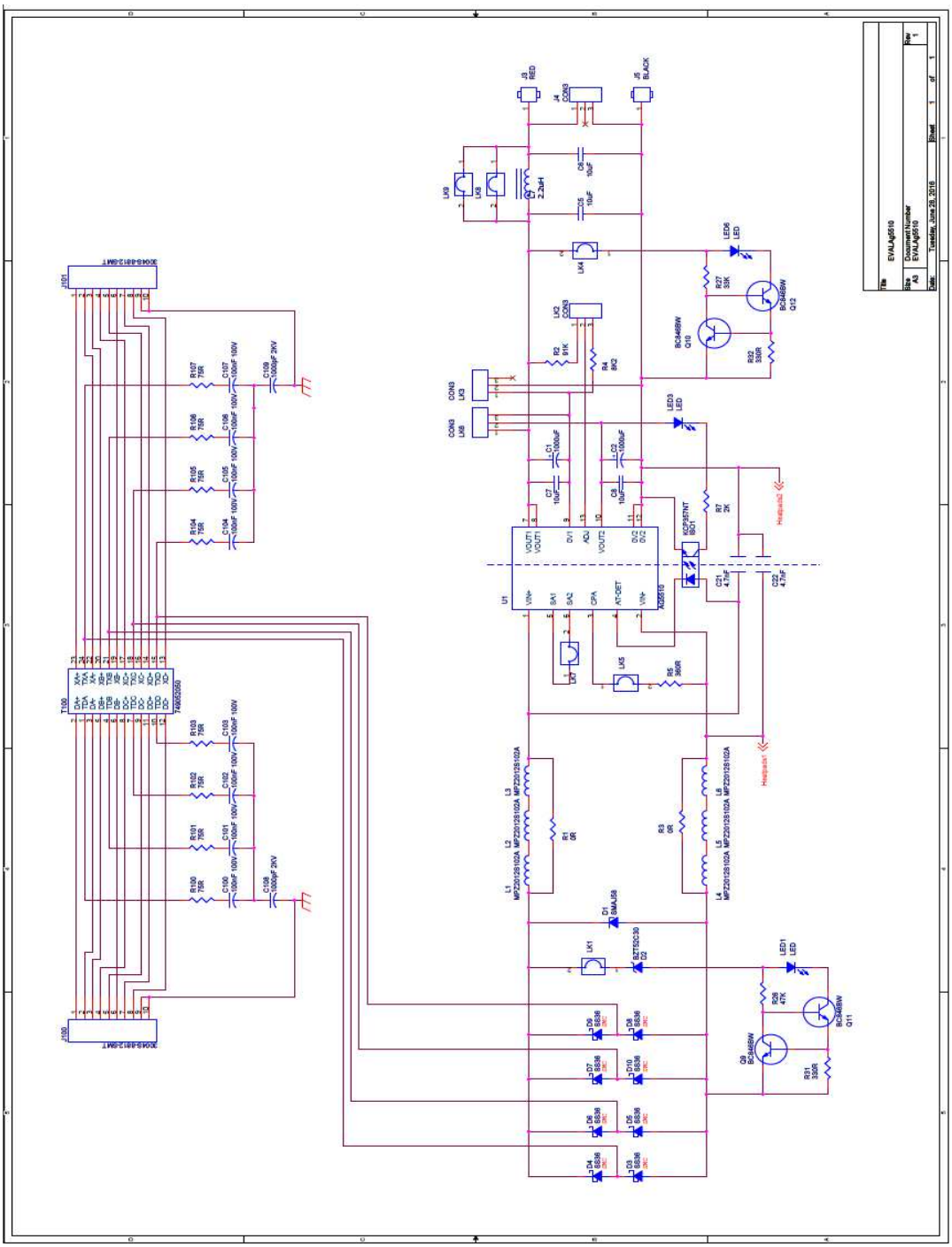

Figure 4: EVALAg5510 1R Schematic

6.3 Link settings

LK1 – Input power LED
LK2 – Output adjust select
LK3 & LK6 – Output configuration (Parallel “12V” or Series “24V”)
LK4 – Output power LED
LK5 – Selects Class 5 programming
LK7 – Signature Adjustment
LK8 & LK9 – Optional Pi Filter