
# POEAg5500 Evaluation Board User Manual

Rev 1.1 – March 2012

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# 3 Introduction

This manual is intended to be a guide to using the “EVALAg5500” (Rev 1R or higher) evaluation board with an Ag5500 Powered Device (PD) module.

The EVALAg5500 evaluation board can be powered using the spare pair in the CAT5e cable (pins 4 & 5 and pins 7 & 8), and / or over the data pair through on-board IEEE802.3at compliant magnetics.

# 4 Board Description

The input data and power is supplied to the board through connector J1. The data is passed through to the peripheral equipment via J2, with the power form the Ag5500 module is supplied via J3 to J7 (see Figure 1 & 4).

The EVALAg5500 on-board bridge rectifiers will ensure that the correct input polarity is applied to the Ag5500.

There are two LED’s that indicates which input is applying the power (the silk screen on the PCB shows which pair SPARE or DATA). These can be disabled by removing the jumper links LK2 (Data) and LK4 (Spare), removing these links does not affect the power being delivered to the Ag5500.

Before using the EVALAg5500 evaluation board, it is important to setup the output configuration jumpers for the product that is going to be use.

## *4.1 Input Signature and Classification*

Phihong have developed a range of POE Ultra Power Sourcing Equipment (PSE) to provide higher power than specified in IEEE802.3at. The signature for this PSE range does not conform to the IEEE802.3af or IEEE802.3at standards. The Ag5500 is designed to work with this range and LK7 will connect the SA1 and SA2 signature adjustment pins. For other PSEs ensure LK7 in not fitted.

The EVALAg5500 evaluation board has a Class 4 programming resistor fitted (R2). LK3 should be fitted to enable Class 4. If LK3 is not fitted then the Ag5500 will default to Class 0.

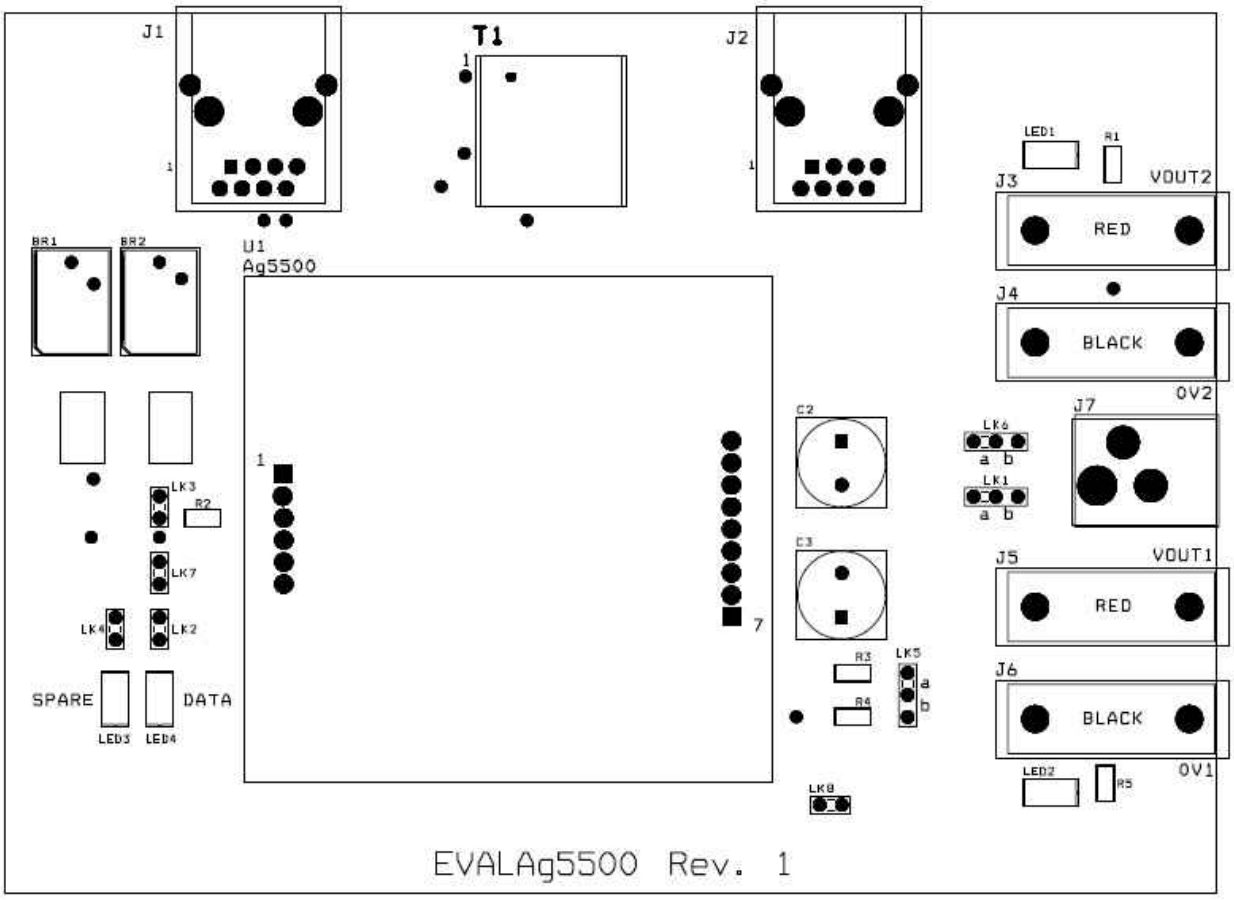


Figure 1: Board Layout

## 4.2 PD Output Selection

The Ag5500 has two DC outputs that must be connected in parallel or in series, the EVALAg5500 board output connections are shown in Table 1: -

| Output | Connections | |
|---|---|---|
| 0V 1 | J6 | J7 (Outer) |
| VOUT 1 | J5 | |
| 0V 2 | J4 | |
| VOUT 2 | J3 | J7 (Centre) |

Table 1: Output Connections

The Ag5500 outputs cannot be run independently, so the EVALAg5500 board has output selector links LK1 and LK6.

For parallel outputs both of these links must be in position “a” - VOUT1 connected to VOUT 2 and 0V 1 connected to 0V 2.

For series outputs both links must be in position “b” – VOUT 1 connected to 0V 2.

The DC10 connector J7 delivers a nominal 12V when the outputs are in parallel and 24V when the outputs are in series (see Table 1 for connections).

## 4.3 Output adjustment

The primary output (VOUT 1 – 0V 1) has an ADJ pin, which allows the output voltage to be increased or decreased from its nominal value. The secondary output (VOUT 2 – 0V 2) will track the adjusted primary output voltage.

The EVALAg5500 board has an adjust link LK5 and two resistors R3 (91K) and R4 (8K2) which allows the output to be adjusted to its maximum and minimum values.

To reduce the output voltage to its minimum level, connect a link to LK5 position “a”. To increase the output voltage to its maximum level, connect a link in position “b”. If the output voltage needs to be set to a different value (within the adjustment range) then connect a resistor instead of a (0R) link.

## 4.4 Minimum Load

The Ag5500 requires a minimum load of 100mA to maintain normal operation. The EVALAg5500 board if fitted with a ~100mA load which can be applied by fitting LK8. If the external load connected to the board always exceeds 100mA, then this link does not need to be fitted.

# 5 Typical Set-up

Figure 2 shows the basic set up using the POE evaluation board with a High Power Midspan or Endspan.

The equipment required: -

- Midspan or Endspan PSE (Power Sourcing Equipment)
- Peripheral (or Test) Equipment
- CAT5e cables
- Output power cable
- Mains cable

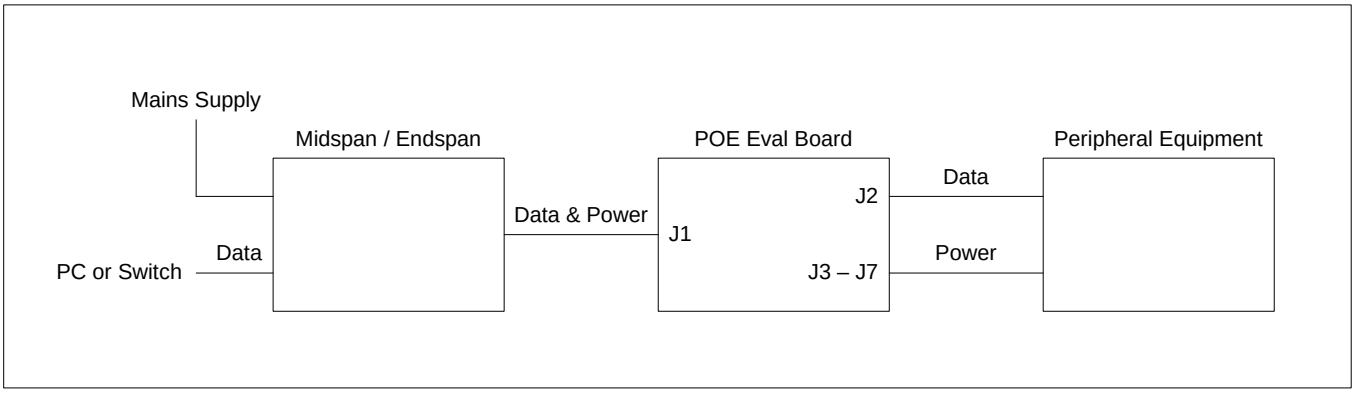


Figure 2: Basic set-up

# 6 Using the Board

## 6.1 Typical Application

Figure 3 shows an example set-up using an Ag5500 powered by a Phihong POE60U-560(G)-SS-R Midspan and supplying +12V to a Vivotek PZ6122 (or PZ6112) ethernet camera.

The PC ethernet port is connected to the data input of the POE60U-560(G)-SS-R (PSE) via a short Cat5e patch cable. The Data & Power output from the POE60U-560(G)-SS-R is connected to the input of the EVALAg5500 evaluation board (J1) via a CAT5e crossover cable. The data output (J2) of the EVALAg5500 evaluation board is connected to the data port of the ethernet camera via a short CAT5e patch cable. The +12V (parallel configuration) power output from the EVALAg5500 evaluation board (J7) connects to the dc input of the Vivotek PZ6122 ethernet camera.

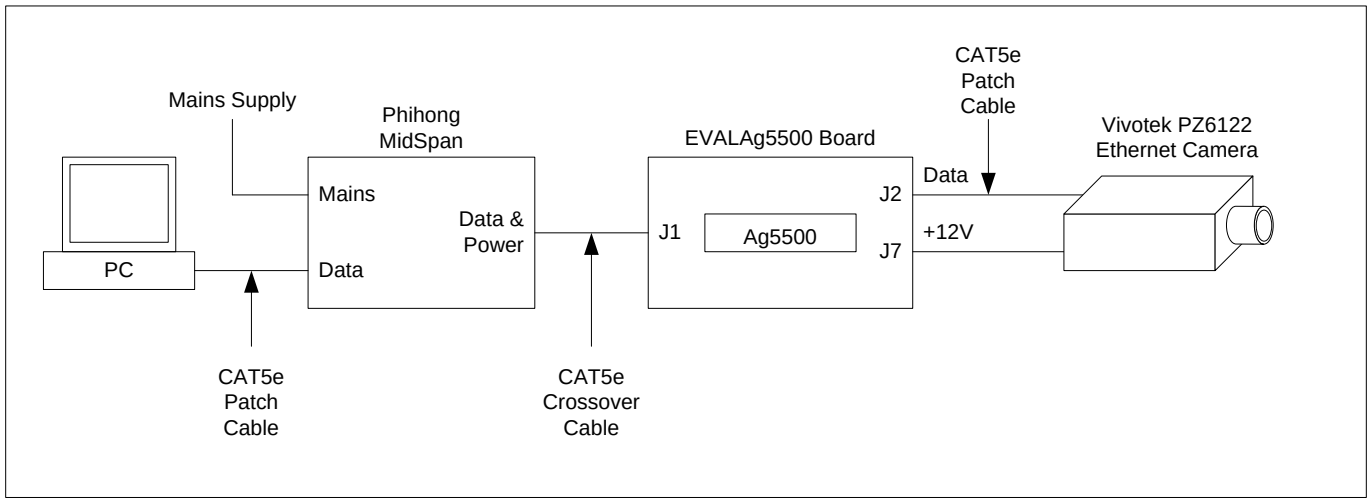


Figure 3: Example set-up

## 6.2 EVALAg5500 Evaluation Board Schematic

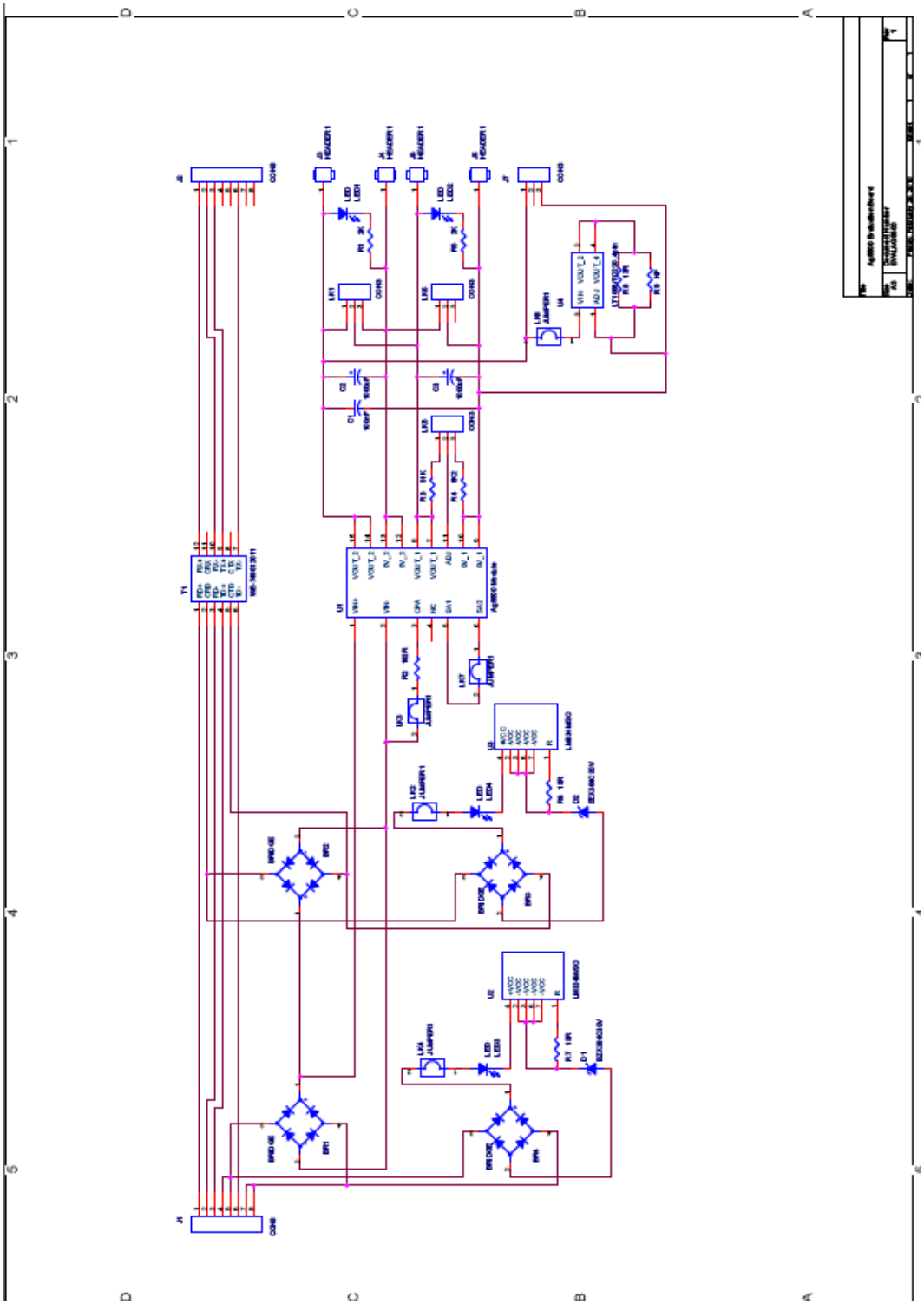

Figure 4: EVALAg5500 1R Schematic

## 6.3 Link settings

LK1 & LK6 – Output configuration (Parallel “a” or Series “b)
LK2 & LK4 – Input power LEDs
LK3 – Selects Class 4 programming
LK5 – Output adjust select (minimum “a” or maximum “b”)
LK7 – Signature Adjustment
LK8 – On-board 100mA load