



**EVALAG5200 Rev 1
Evaluation Board User
Manual**

Rev 1.0 – January 2013

1 Table of Contents

1	Table of Contents	1
2	Table of Figures	1
3	Introduction	2
4	Board Description	2
	4.1 <i>Input Selection and Classification</i>	2
	4.2 <i>Output adjustment</i>	3
5	Typical Set-up	4
6	Using the Board	5
	6.1 <i>Typical Application</i>	5
	6.2 <i>EVALAG5200 REV 1R - Evaluation Board Schematic</i>	6
	6.3 <i>Link settings</i>	6

2 Table of Figures

Figure 1:	Board Layout.....	3
Figure 2:	Basic set-up	4
Figure 3:	Example set-up	5
Figure 4:	Board Schematic.....	6

3 Introduction

This manual is intended to be a guide to using the “EVALAG5200 Rev1.0” evaluation board with a Silvertel Ag5200 Powered Device (PD) module.

4 Board Description

The input data and power is supplied to the board through connector J1. The data is passed through to the peripheral equipment via J2, with the power from the PD module is supplied via J3 to J5 (see Figure 1 & 4).

The EVALAG5200 on-board bridge rectifiers will ensure that the correct input polarity is applied to the PD.

4.1 Input Selection and Classification

The EVALAG5200 board will automatically direct the power from J1 to the Ag5200's input. LED2 will be illuminated when PoE power is being applying to the board. LK1 can be removed if you do not want LED2 to illuminate.

The Ag5200 Classification is fixed at Class 4 and does not need any external programming components.

When the EVALAG5200 board is connected to an IEEE802.3at (PoE+) compliant PSE such as a Pihong POE36U-1AT-R; the PSE will detect Class 4 and output 2-Event classification pulses. In turn the Ag5200 detects these pulses and activates the AT-DET detect output. This output is connected to an opto-isolator to cross the isolation barrier and LED 3 will be illuminated.

Note: The EVALAG5200 does not have an on-board PHY or μ -controller; so does not perform the Data Link Layer (DLL) classification communications back to the PSE (to confirm its power requirement). Many IEEE802.3at PSEs (such as the Pihong POE36U-1AT-R) do not need this and will automatically supply full Type 2 power at start-up. But there are several Switches (e.g. Cisco) that will only output Type 1 power level (<15.4W), until they receive DLL confirmation that the PD is Type 2 and supports the higher power level.

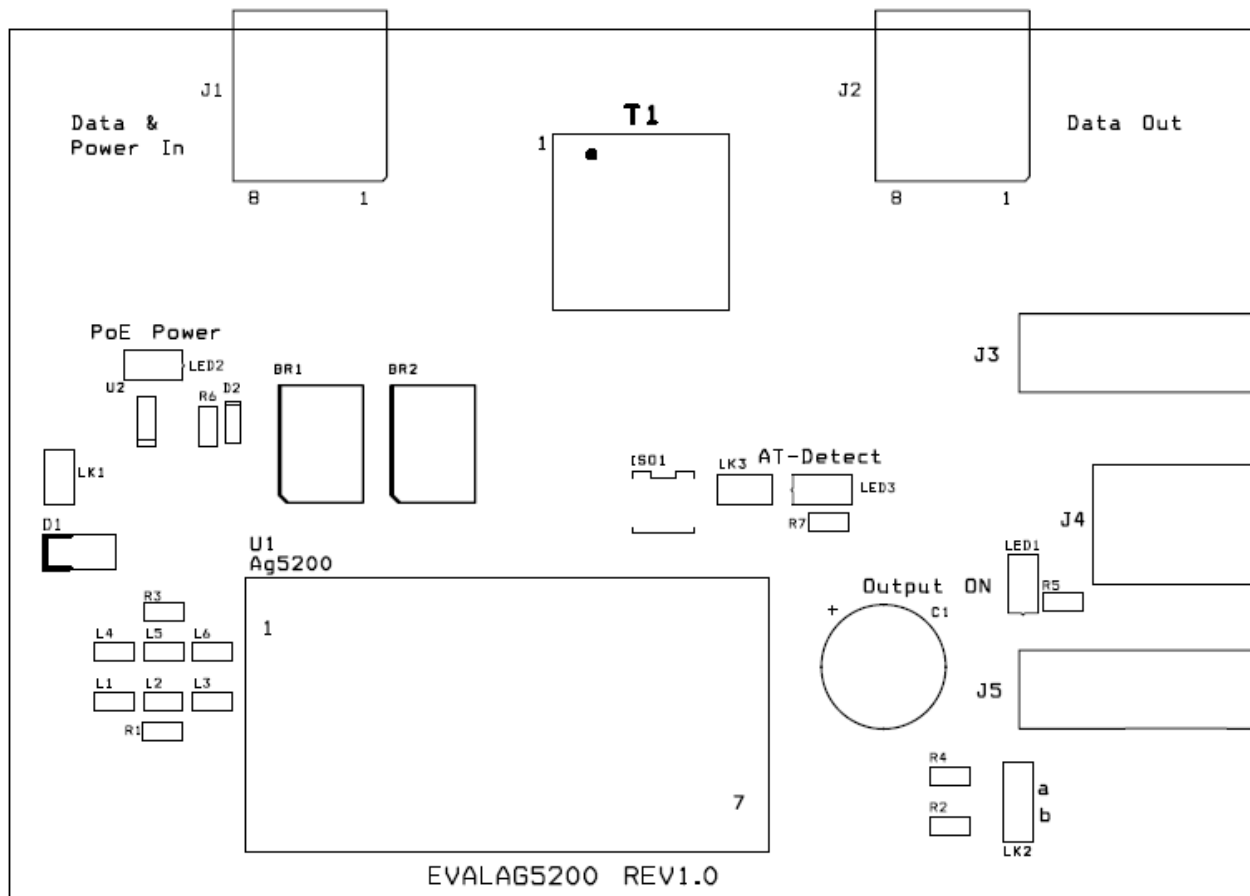


Figure 1: Board Layout

4.2 Output adjustment

The Ag5200 output has an ADJ pin, which allows the output voltage to be increased or decreased from its nominal value.

The EVALAG5200 board has an adjust link LK2 and two resistors R2 (100K) and R4 (0R) which allows the Ag5200 output to be adjusted to its maximum and minimum values.

To increase the output voltage (to its maximum) connect a link to LK2 position in “a”; to reduce the output voltage (to its minimum) connect a link in position “b”. If the output voltage needs to be set to a different value (within the adjustment range) then connect a resistor instead of a (0R) link.

5 Typical Set-up

Figure 2 shows the basic set up using the EVALAG5200 evaluation board with a Midspan or Endspan.

The equipment required: -

- Midspan or Endspan PSE (Power Sourcing Equipment)
- Peripheral (or Test) Equipment
- CAT5e cables
- Output power cable
- Mains cable

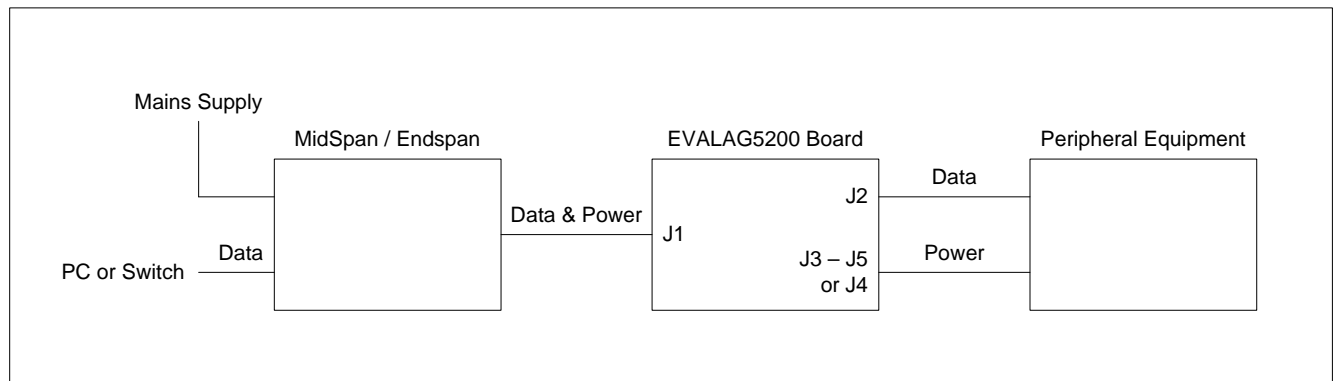


Figure 2: Basic set-up

6 Using the Board

6.1 Typical Application

Figure 3 shows an example set-up using an Ag5200 powered by a Pihong POE36U-1AT-R Midspan and supplying +12V to a Vivotek PZ6122 (or PZ6112) ethernet camera.

The PC ethernet port is connected to the data input of the Pihong POE36U-1AT-R (PSE) via a short Cat5e patch cable. The Data & Power output from the Pihong POE36U-1AT-R is connected to the input of the EVALAG5200 evaluation board (J1) via a CAT5e crossover cable (up to 100m). The data output of the EVALAG5200 evaluation board is connected to the data port of the ethernet camera via a short CAT5e patch cable. The +12V (parallel configuration) power output from the EVALAG5200 evaluation board (J4) connects to the dc input of the Vivotek PZ6122 ethernet camera.

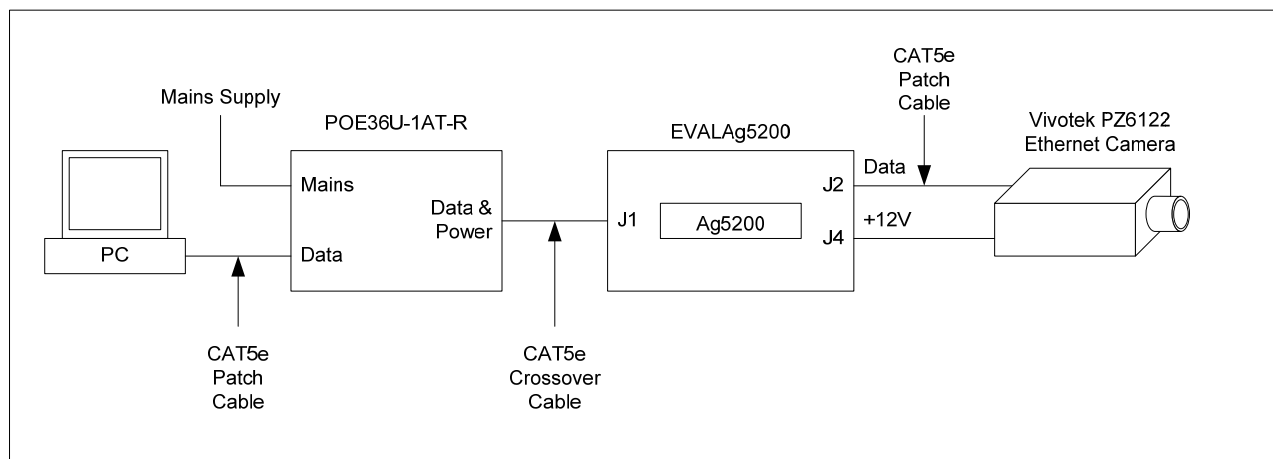


Figure 3: Example set-up

6.2 EVALAG5200 REV 1R - Evaluation Board Schematic

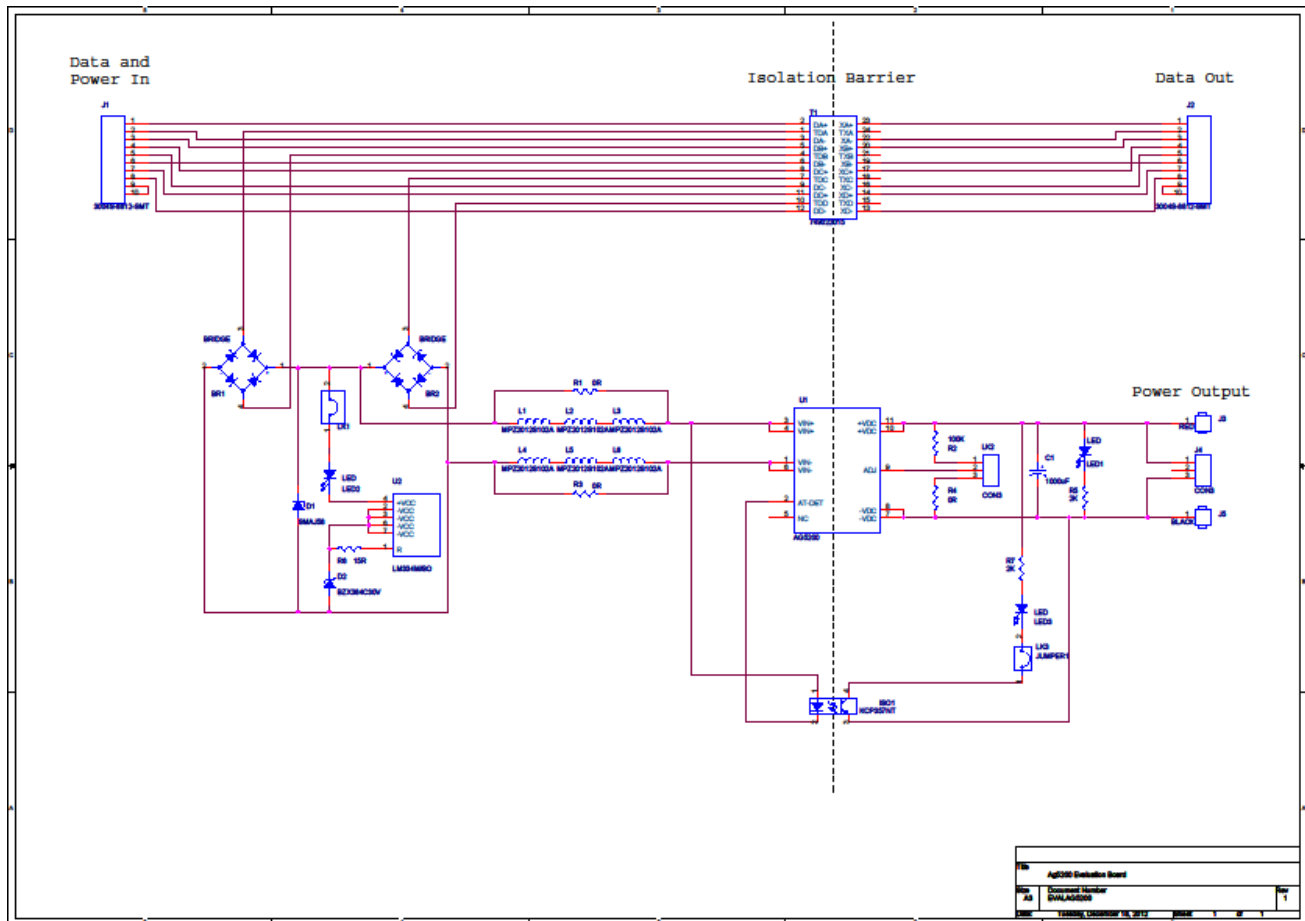


Figure 4: Board Schematic

6.3 Link settings

- LK1 – Connects input power LED circuit
- LK2 – Output adjust select
- LK3 – IEEE802.3at PSE detection LED